

Sideswipe&Jazz AMD2 Logic Schematics

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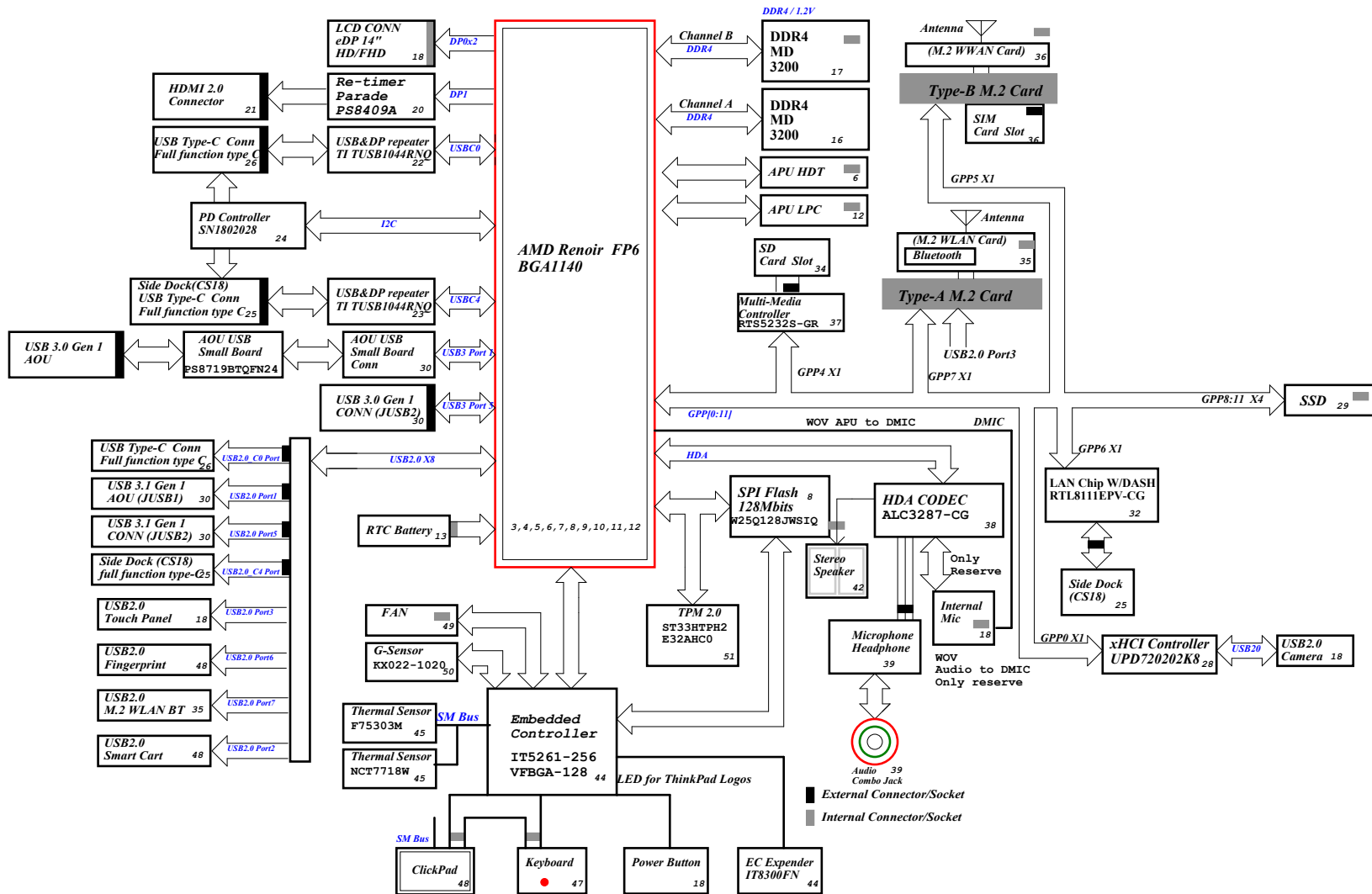
064_DC/DC+1.2VP(RT8231)

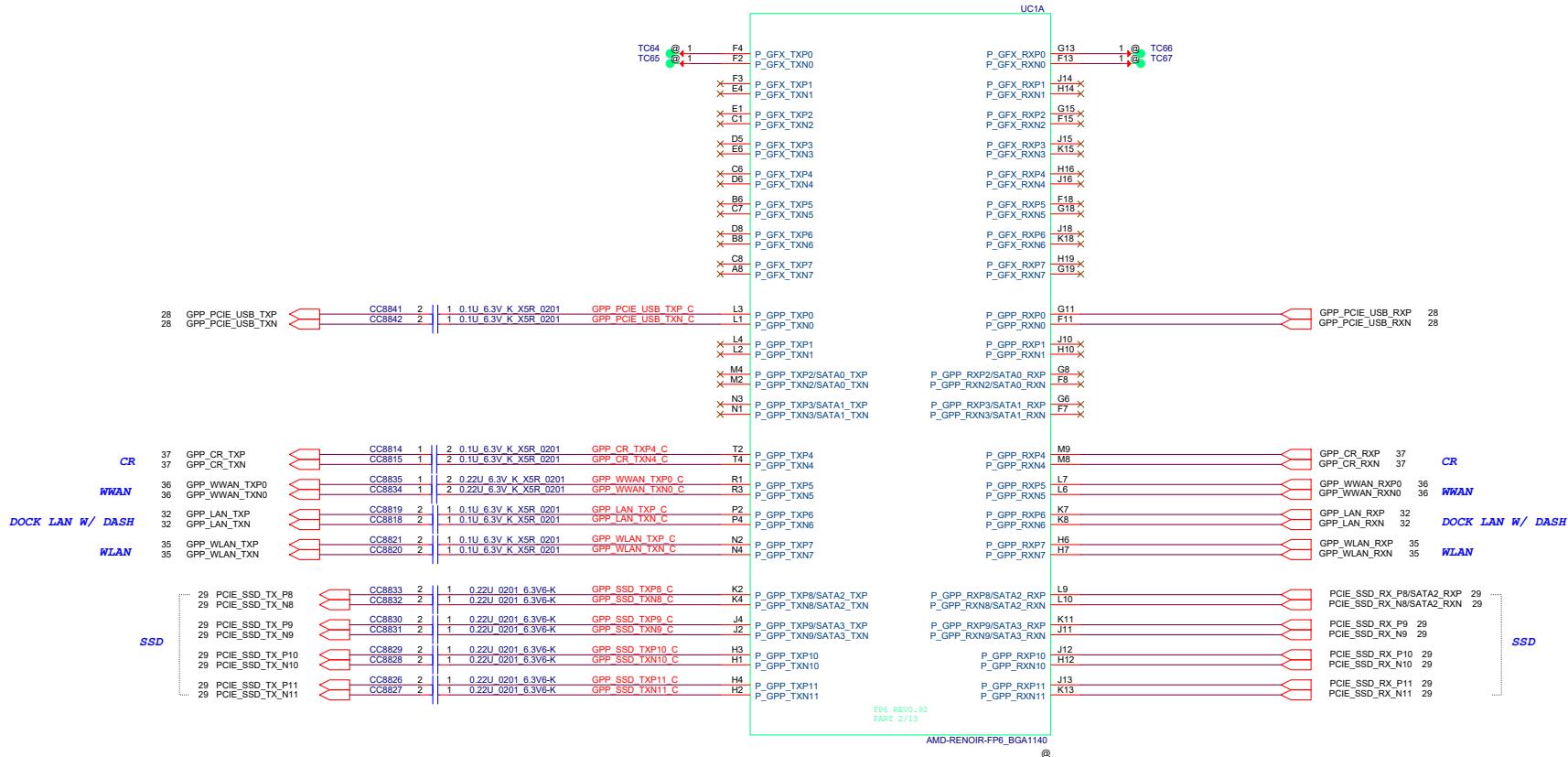
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066_DC/DC_+1.8VALW (NB691)

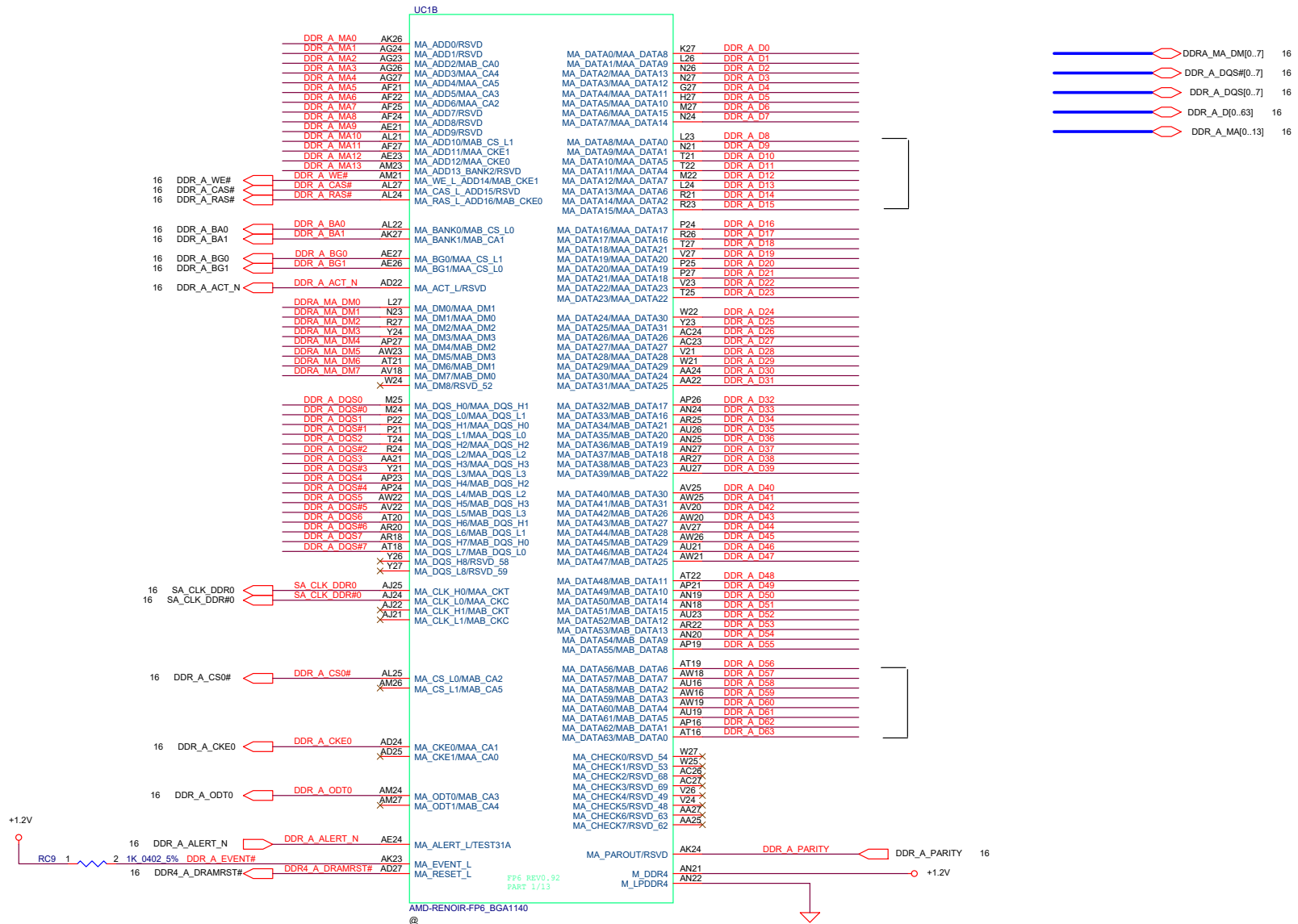
067_PWR-Power Diagram

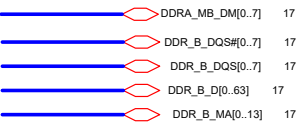
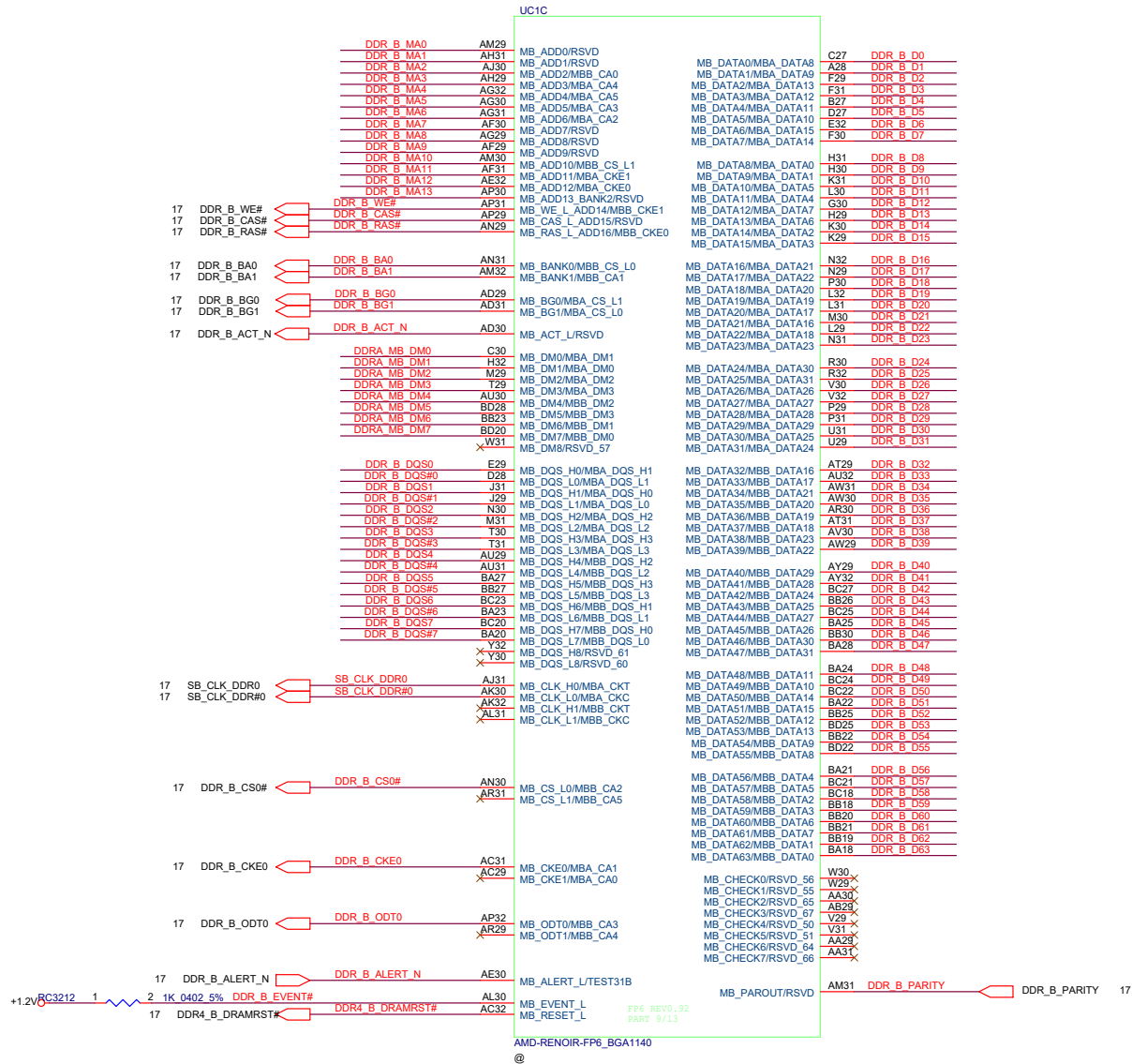
068_SCREW






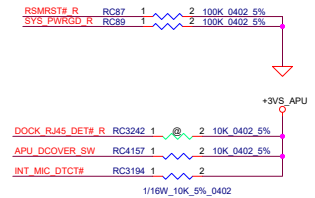
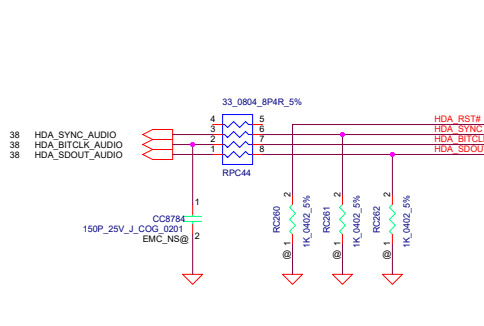
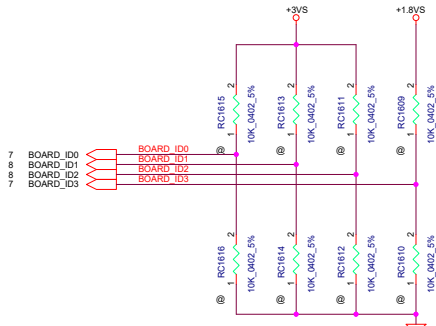
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2018/8/9		2018/8/9		2018/8/9	
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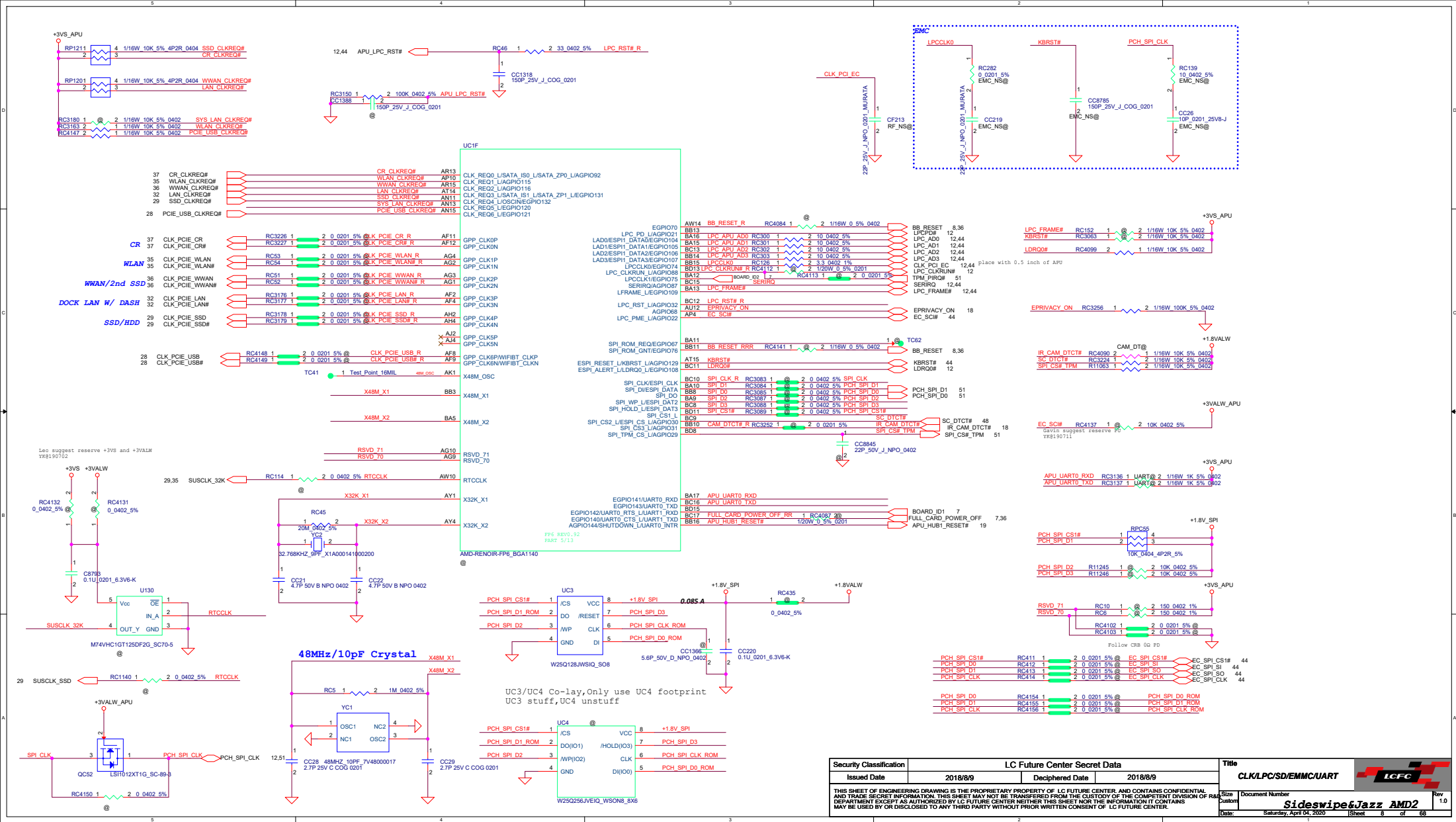


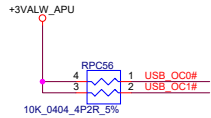


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Board ID	Description	Stuff R
Board ID (3, 2, 1, 0)	0000 Samsung 8Gb 3200 MT/s	RC1610 RC1612 RC1614 RC1616
	0001 Hynix 8Gb 3200 MT/s	RC1610 RC1612 RC1614 RC1615
	0010 Micron 8Gb 3200 MT/s	RC1610 RC1612 RC1613 RC1616
	0011 Samsung 16Gb 3200 MT/s	RC1610 RC1612 RC1613 RC1615
	0100 Hynix 16Gb 3200 MT/s	RC1610 RC1611 RC1614 RC1616
	0101 Micron 16Gb 3200 MT/s	RC1610 RC1611 RC1614 RC1615
	0110 Samsung 32Gb 3200 MT/s	RC1610 RC1611 RC1613 RC1616
	0111 Micron 32Gb 3200 MT/s	RC1610 RC1611 RC1613 RC1615
	1000 Hynix 32Gb 3200 MT/s	RC1609 RC1612 RC1614 RC1616







TYPE C W/DP

TYPE A AOU

USB HUB1

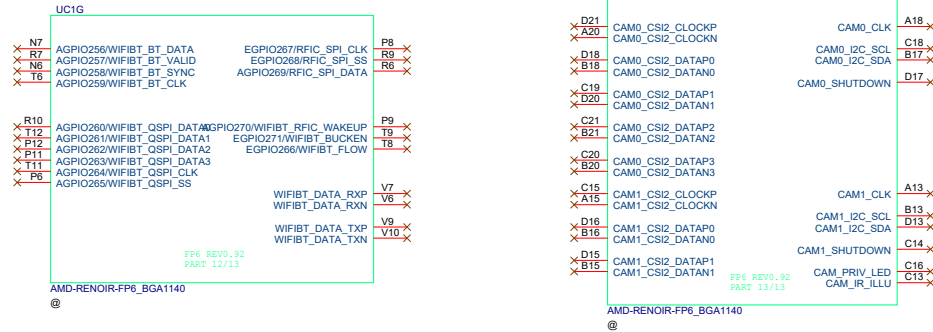
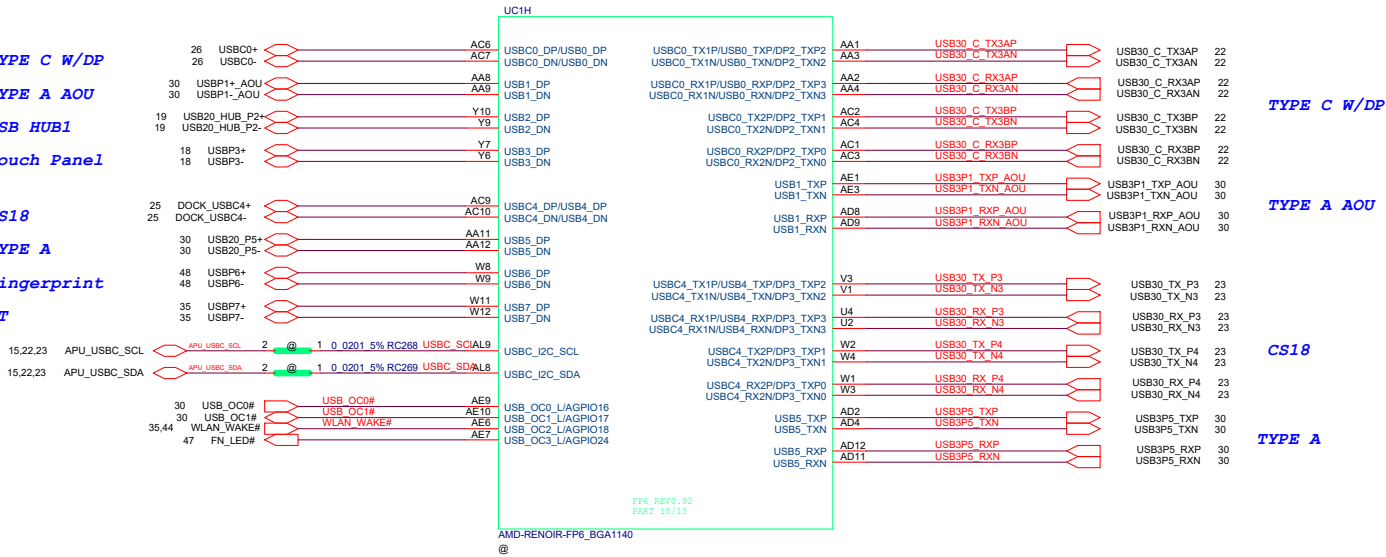
Touch Panel


CS18

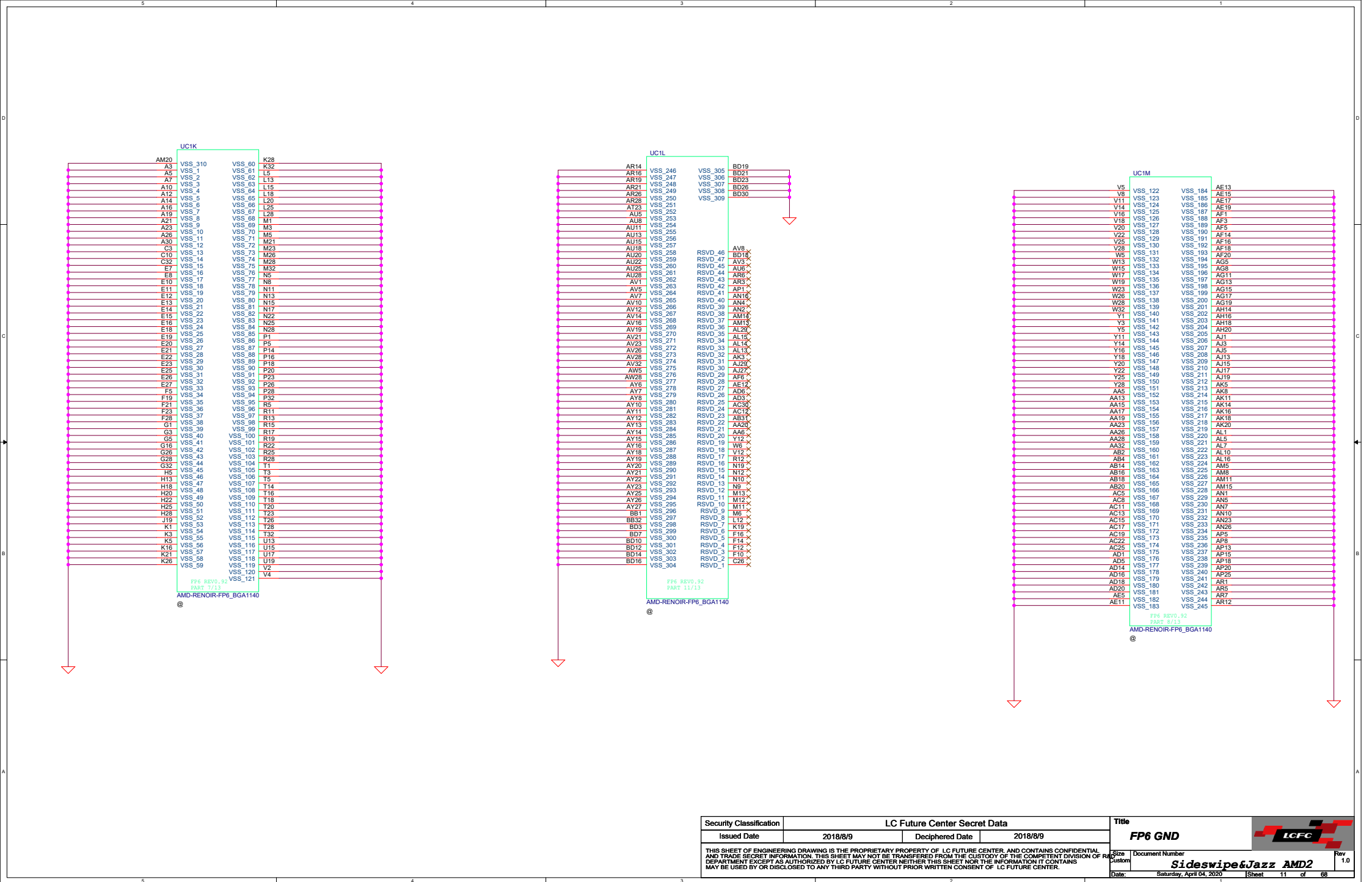
TYPE A

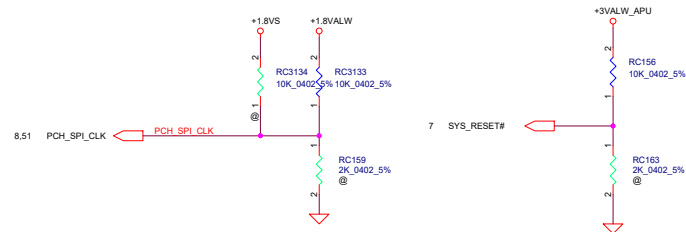
Fingerprint

BT



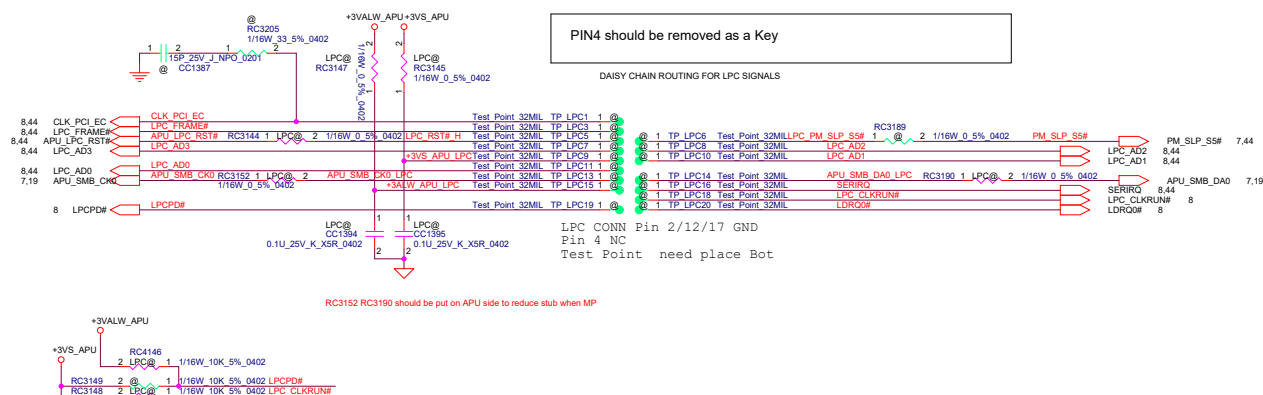
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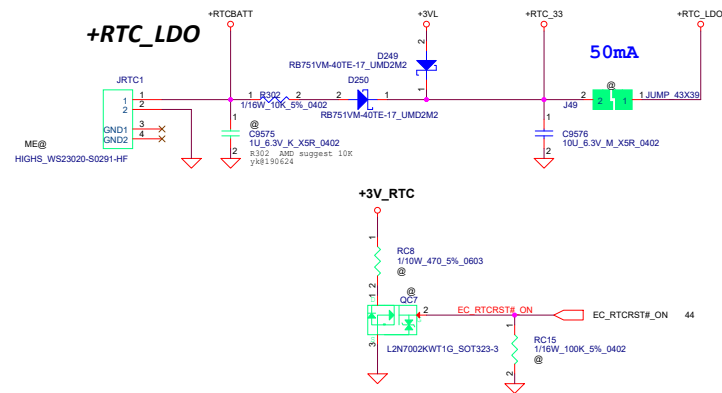




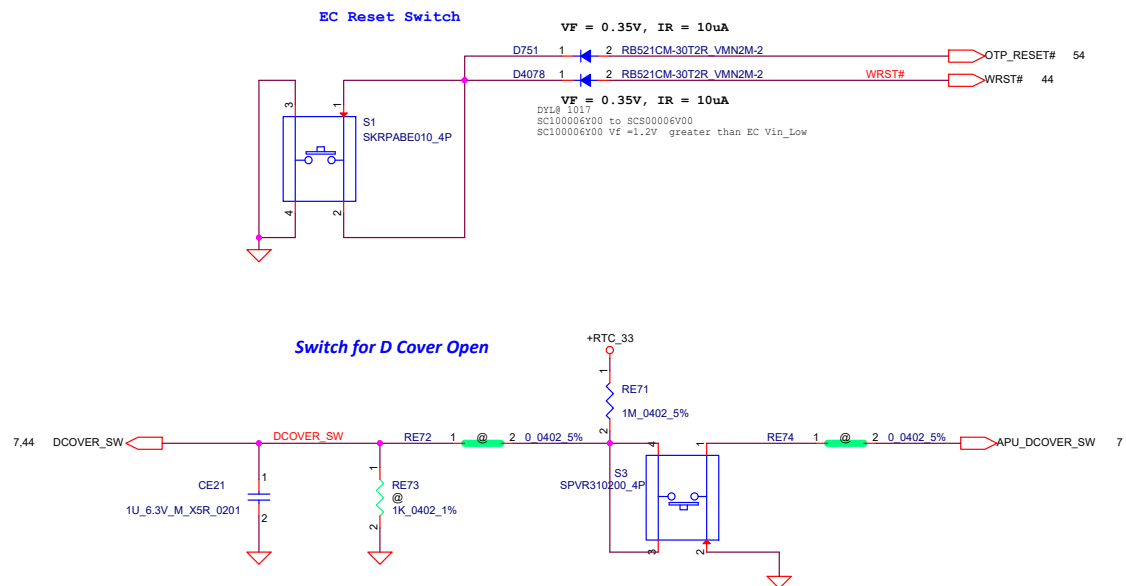
STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

LPC ROM EMULATOR HEADER





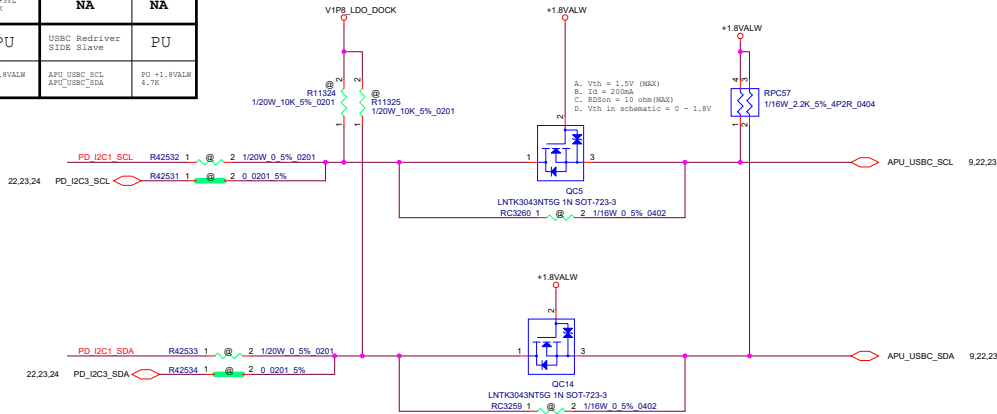
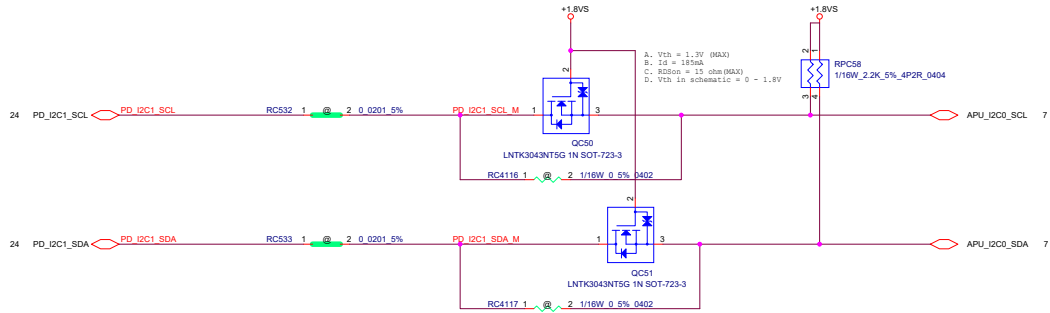
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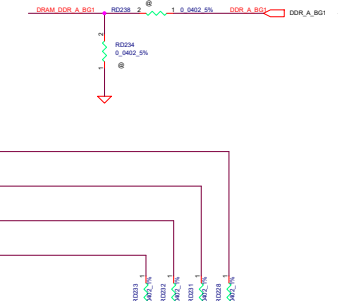
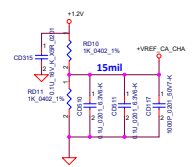


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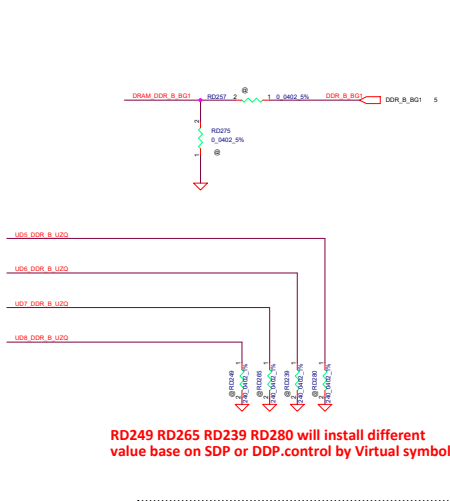
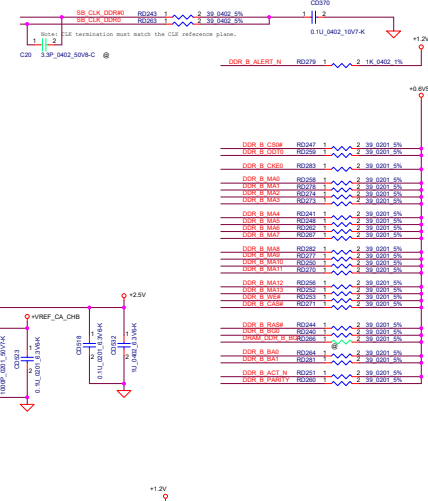
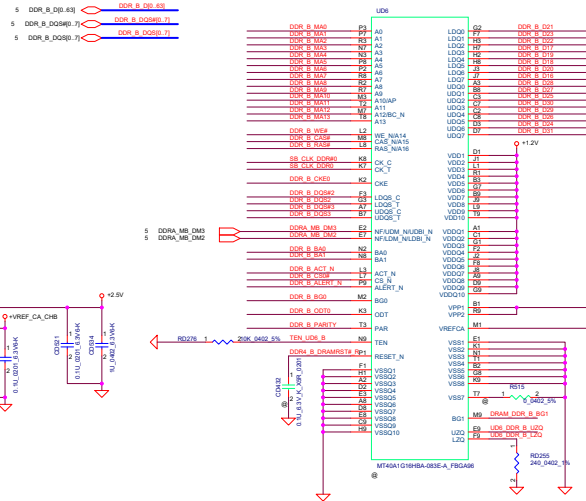
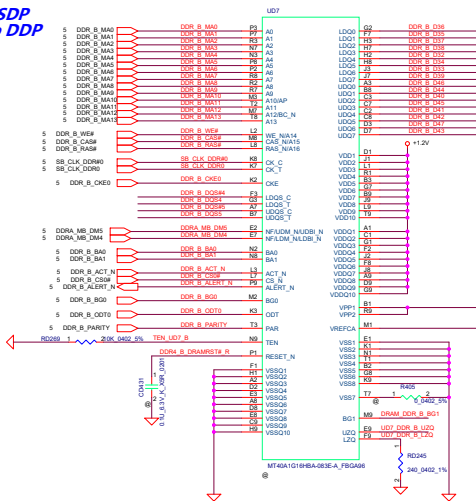
I2C1	Level Shift	PD SIDE I2C1 Slave	PU	APU SIDE I2C0 Master	PU	NA	NA
PD update FW	QC50 QC51	PD I2C1_SCL PD I2C1_SDA	PU VIO3_LDO_DOCK 4.7K	APU I2C0_SCL APU I2C0_SDA	PU 1.8VFS 2.2K	NA	NA
I2C2	Level Shift	PD SIDE I2C2 Slave	PU	EC SIDE Smbus2 Master	PU	NA	NA
PD to EC	NA	PD I2C2_SCL_R PD I2C2_SDA_R	PU +3VL 4.7K	EC SMB_CLK EC SMB_DATA	PU +3VL 4.7K	NA	NA
I2C3	Level Shift	PD SIDE I2C3 Master	PU	APU SIDE USB_C I2C Slave	PU	USBC Redriver SIDE Slave	PU
PD for USBC redriver and APU Mux	QC14 QC5	PD I2C3_SCL_R PD I2C3_SDA_R	PU VIO3_LDO_DOCK 4.7K	APU USBC_SCL APU USBC_SDA	PU +1.8VALW 4.7K	APU USBC_SCL APU USBC_SDA	PU +1.8VALW 4.7K



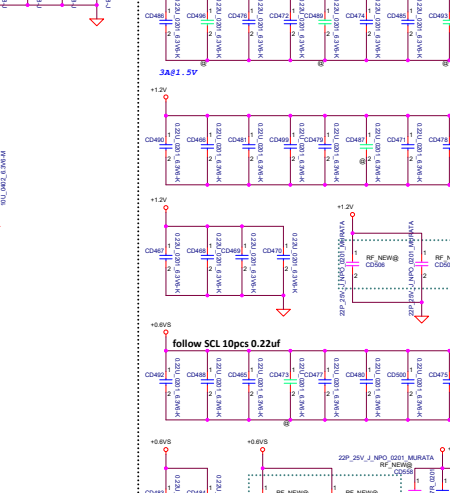
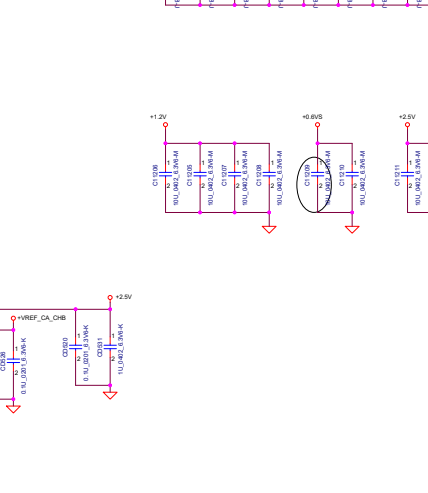
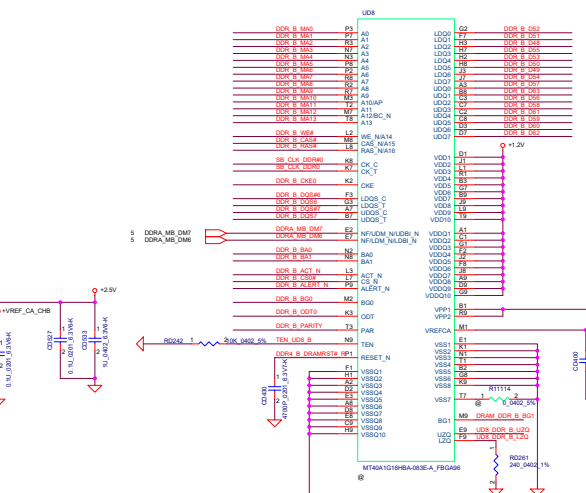
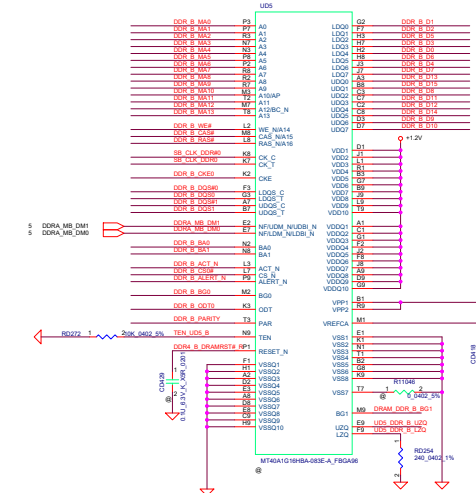
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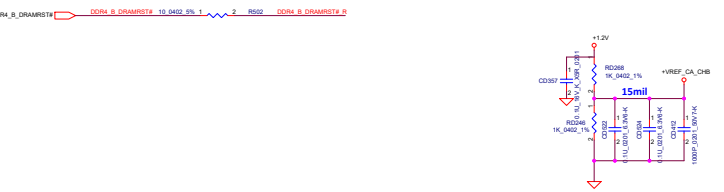
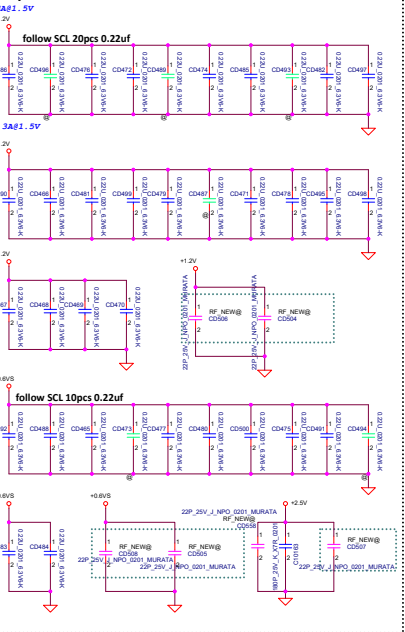
8Gb SDP
16Gb DDP



RD249 RD265 RD239 RD280 will install different value base on SDP or DDP.control by Virtual symbol

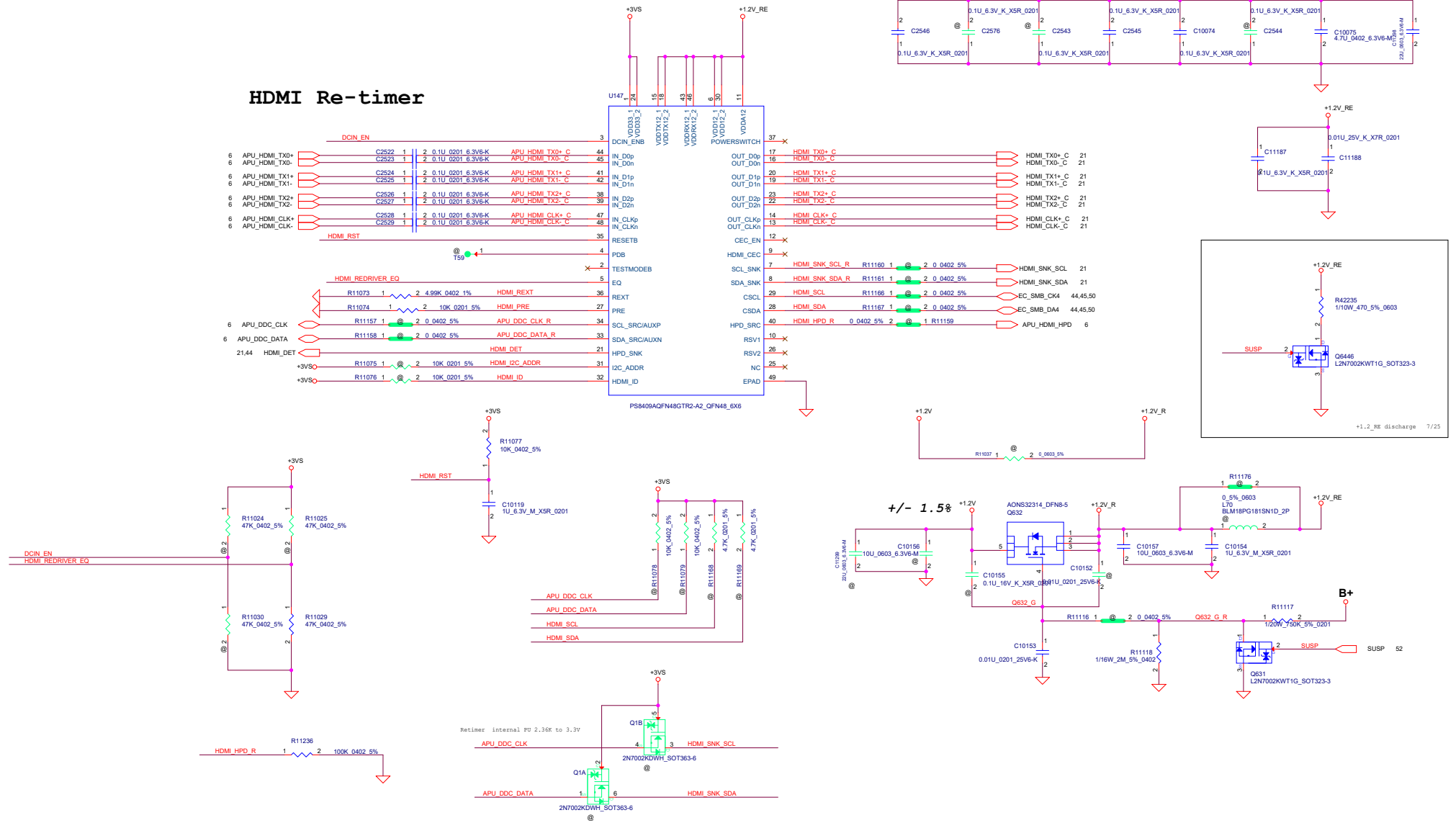


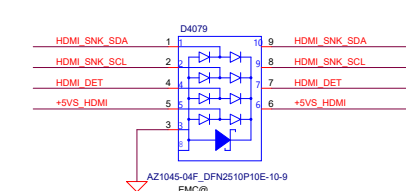
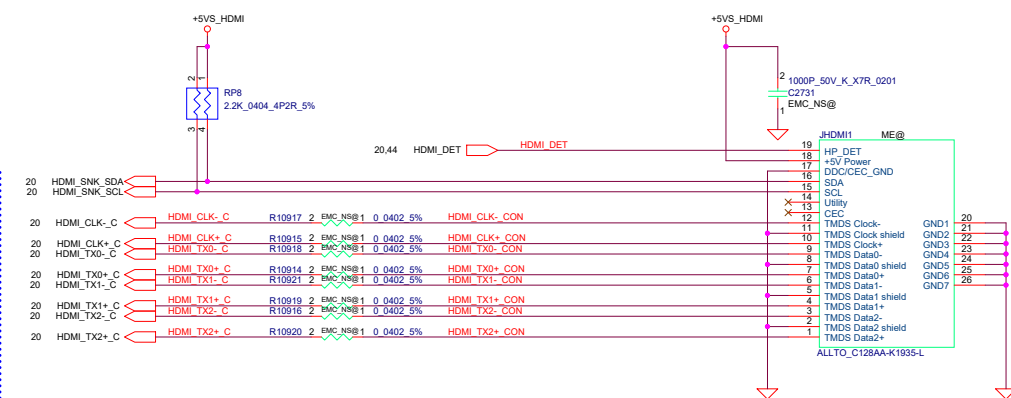
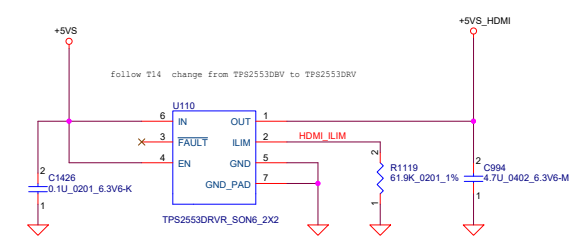
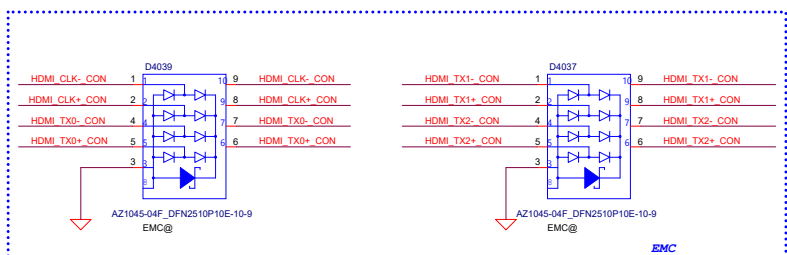
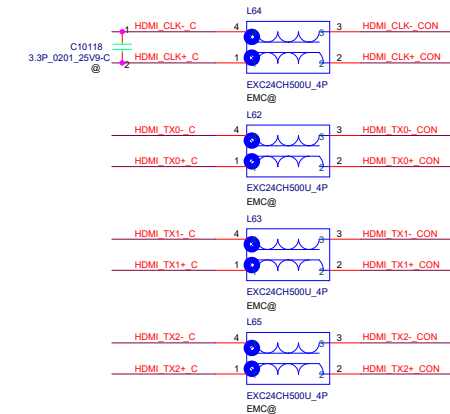
Layout Note: Place near DRAM

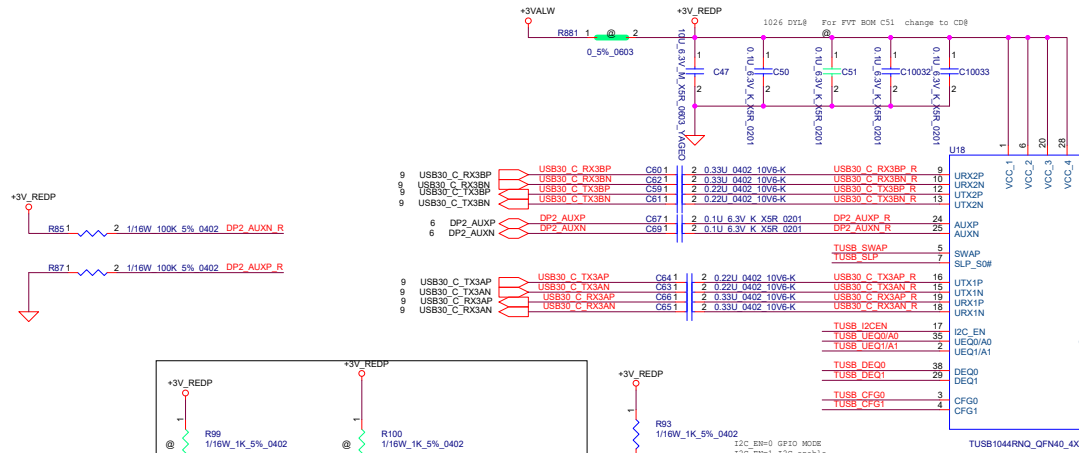


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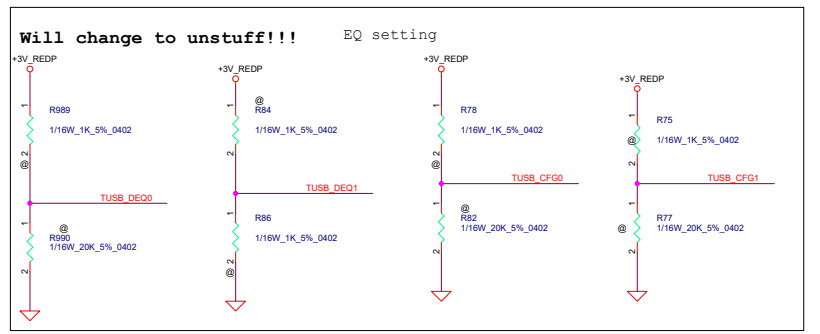
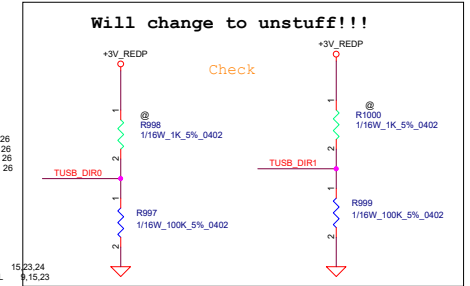
HDMI Re-timer



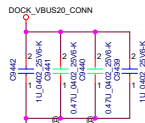
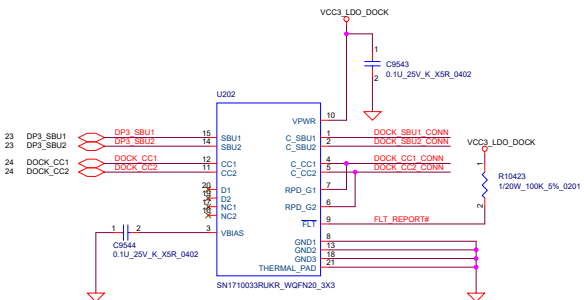




L = DisplayPort Disabled.
H = DisplayPort Enabled.
When I2C_EN = 0, this pin is not used by device.



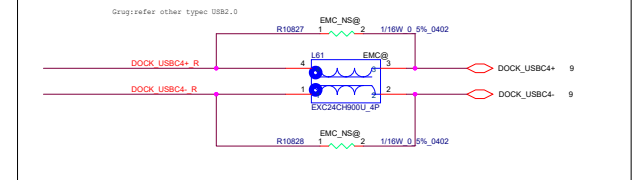
This PIN selects I/O voltage levels for the 2-level GPIO and I2C
0 = 3.3-V configuration I/O voltage, 3.3-V I2C interface (Default)
R = 3.3-V configuration I/O voltage, 1.8-V I2C interface
F = 1.8V configuration I/O voltage, 3.3-V I2C interface
1 = 1.8-V configuration I/O voltage, 1.8-V I2C interface



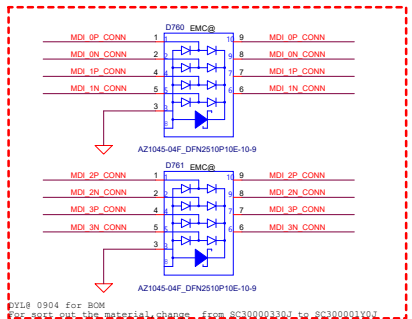
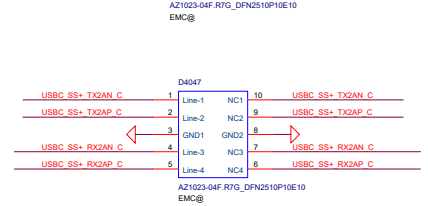
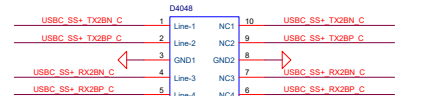
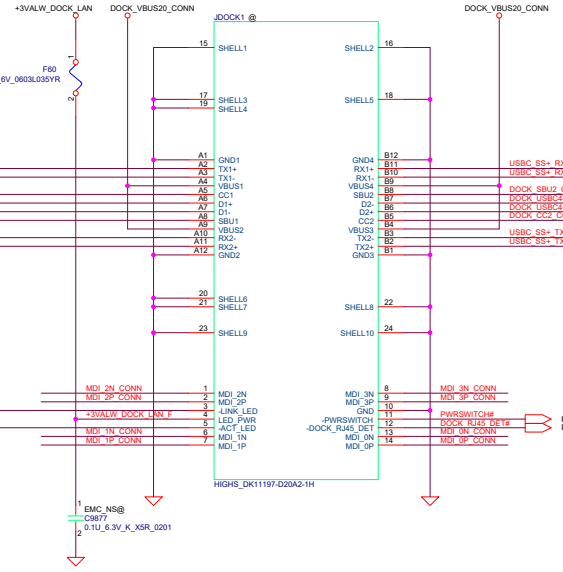
Vendor	P/N	LCFC P/N
KOA	100 +5% 0603	SD000022U0T
Rohm	100 +5% 0603	SD000022V0T
Q269		
Vendor	P/N	LCFC P/N
ON-semi	2N7002KW	SB00001JY00
NXP	NX7002BKW	SB00001GU00

SEL	OE#	V+	V-
X	B	RL-C	RL-C
L	L	M+	M-
R	L	D+	D-

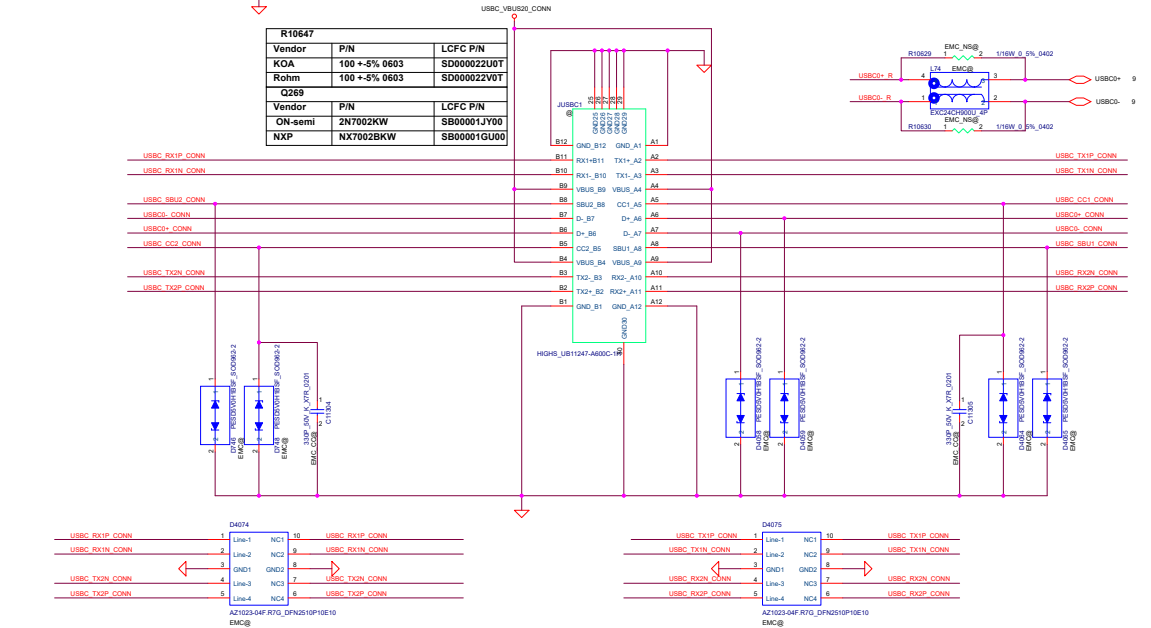
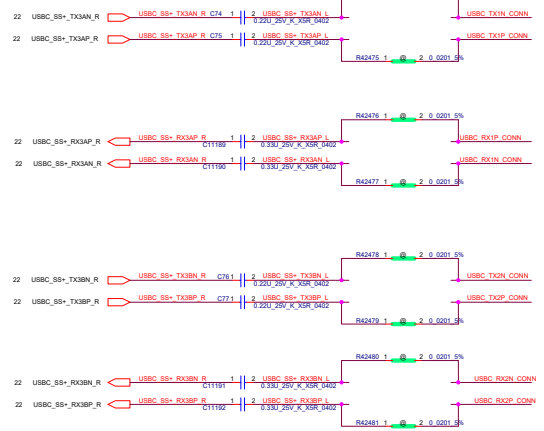
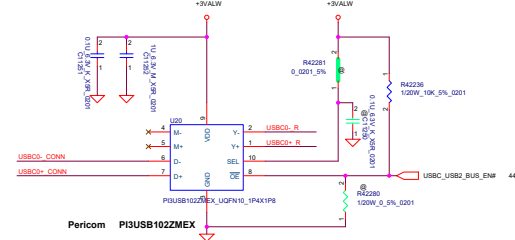
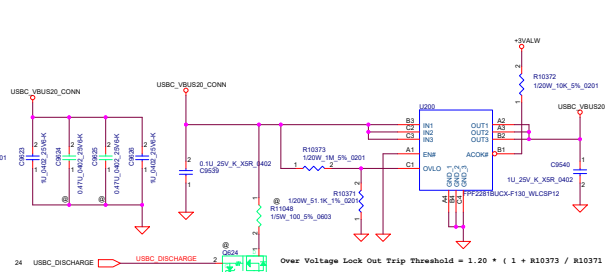
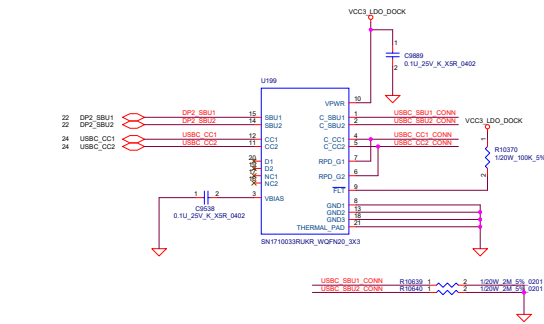
Pericom PI3USB102ZMEX




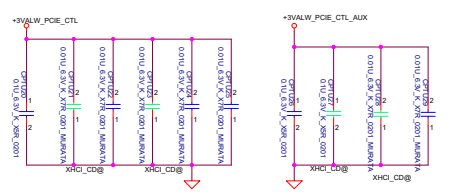
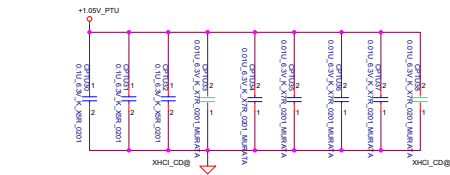
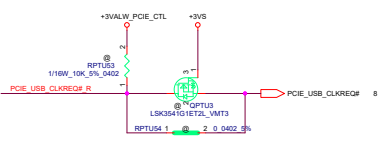
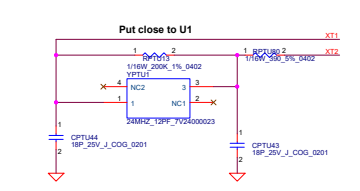
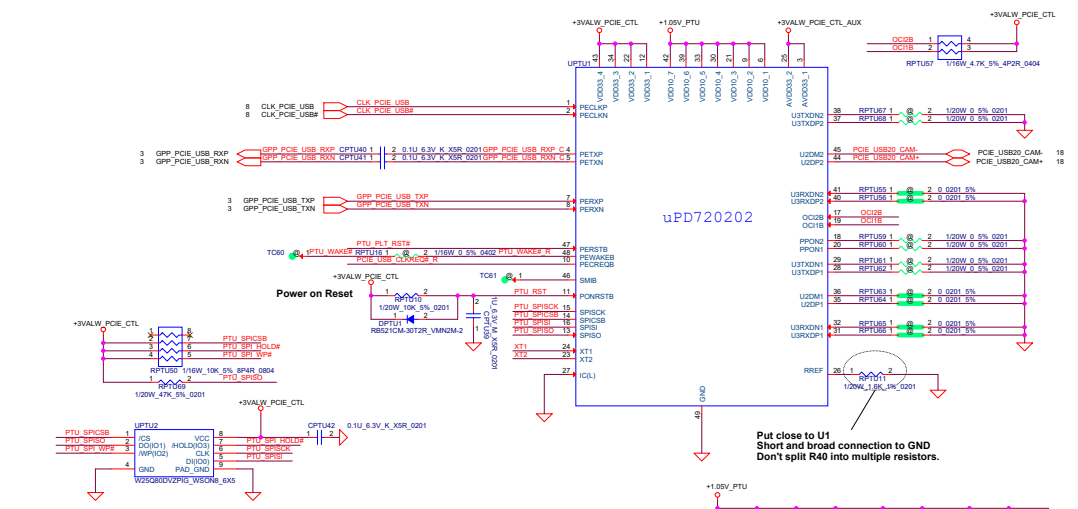
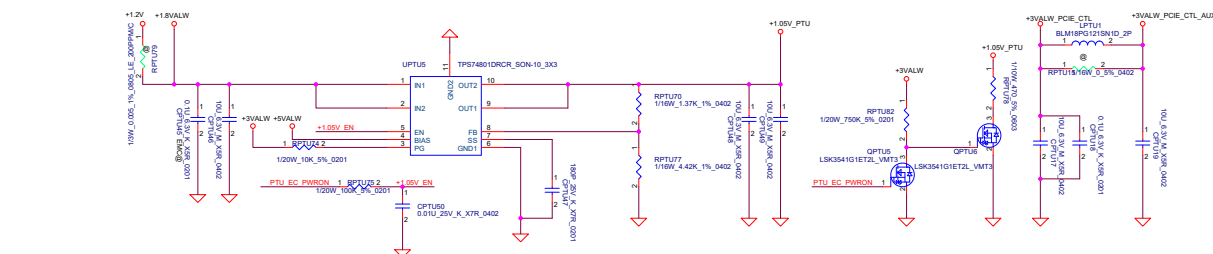
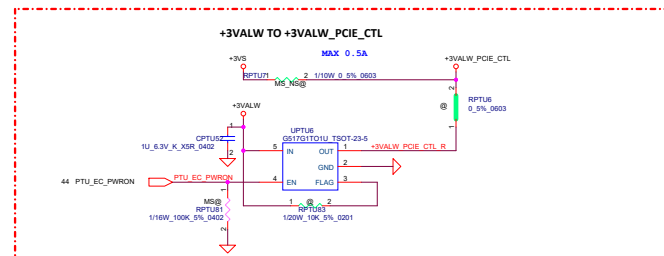
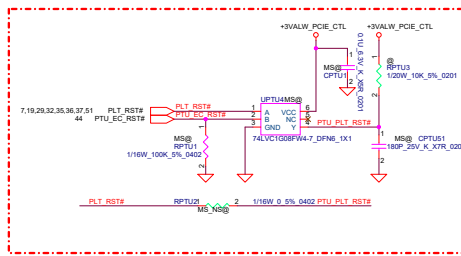
F60		
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AEM	PMS0603-035	SP040007B00

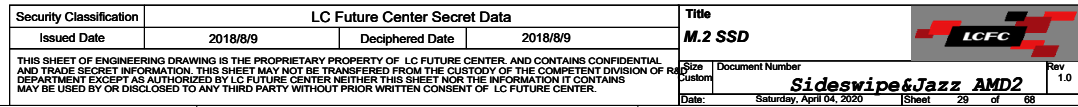
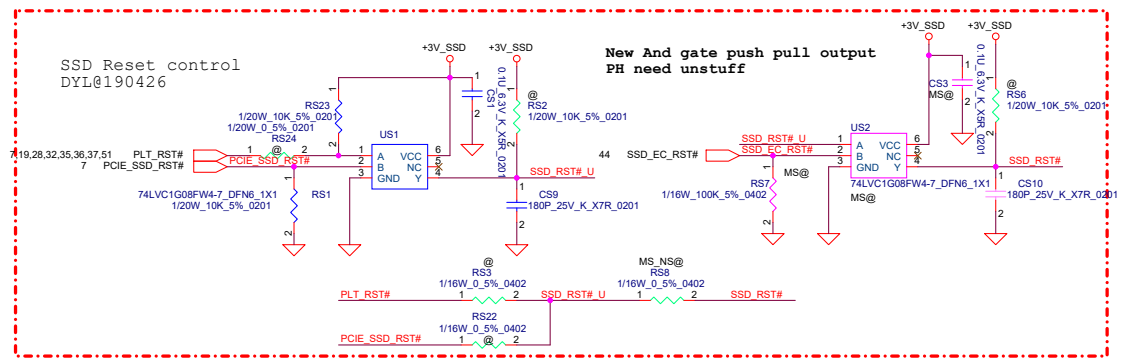


L56 - L59		
Vendor	P/N	LCFC P/N
1st: Murata	DLP11SN900HL2	SM070002Y00
2nd: TDK	MCZ1210AH900L2TA0G	SM070004A00



Security Classification	LC Future Center Secret Data			Title	
Issued Date	2018/8/9	Deciphered Date	2018/8/9		
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Date: Saturday, April 04, 2020				Sheet 27 of 68	





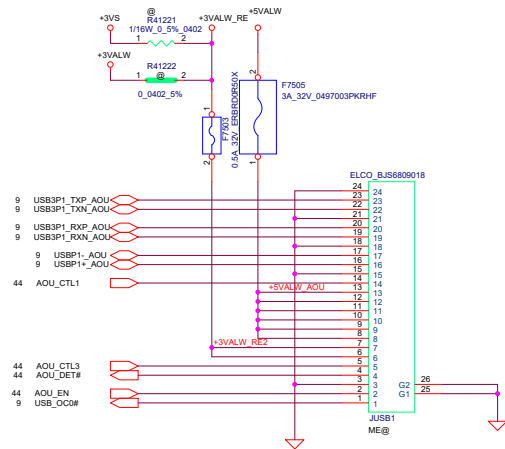
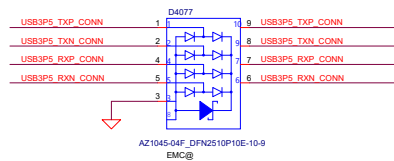
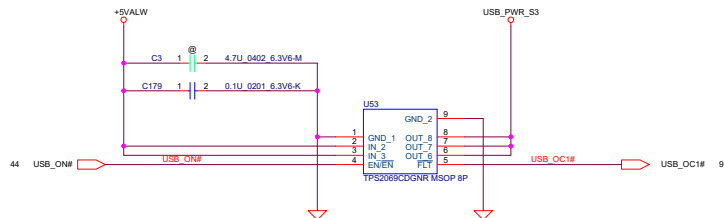
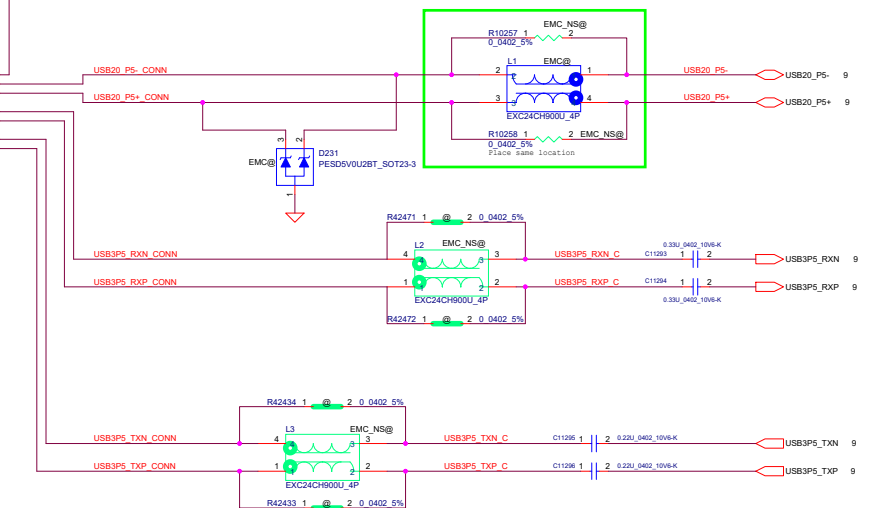
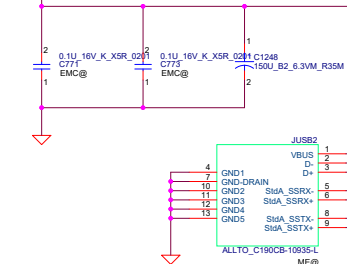


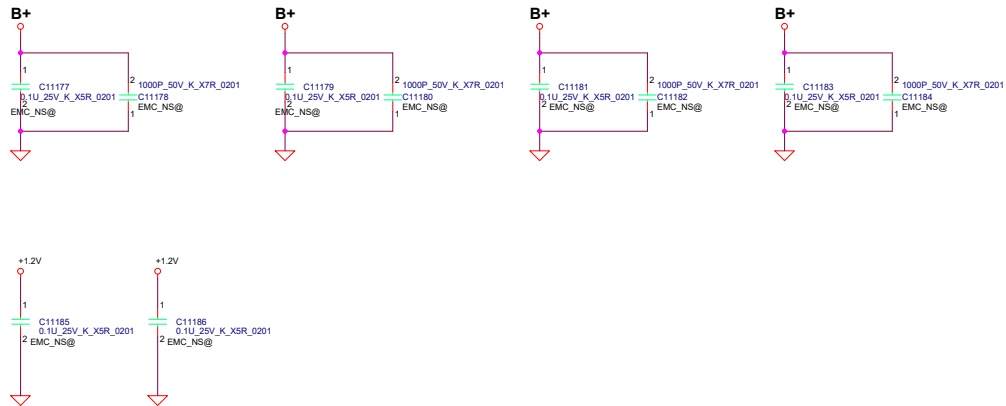
TABLE of USB3.0 Single (U53)		
Vendor	P/N	LCFC P/N
TI	TPS2069CDGNR	SA00005TE00
Rohm	BD82032FVJ-GE2	SA000084S00



USB_PWR_S3
WIDE PATTERN(MIN 500mA)
PLACE NEAR USB CONN



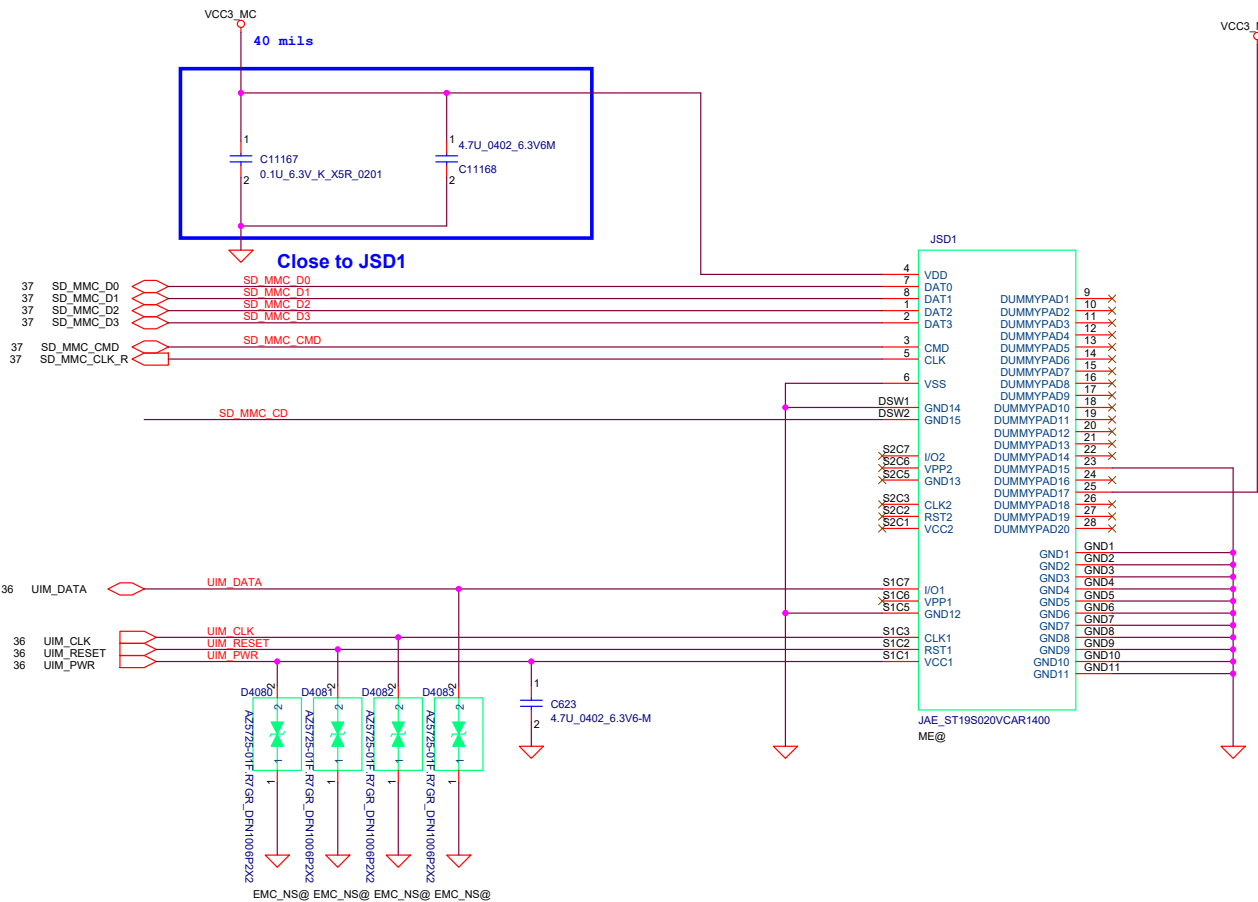
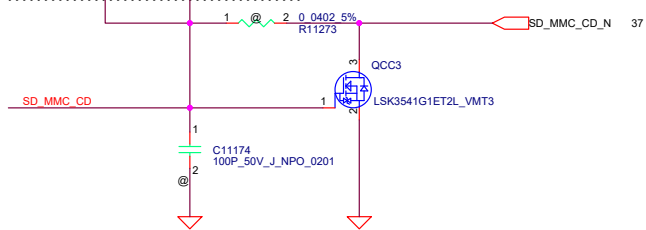
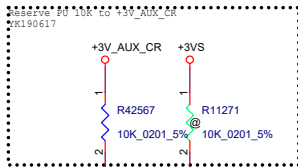
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/8/9	Deciphered Date	2018/8/9	USB POWER/CONN	
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				Custom	1.0
				Date	Rev
				Saturday, April 04, 2020	1.0
				Sheet	30 of 68

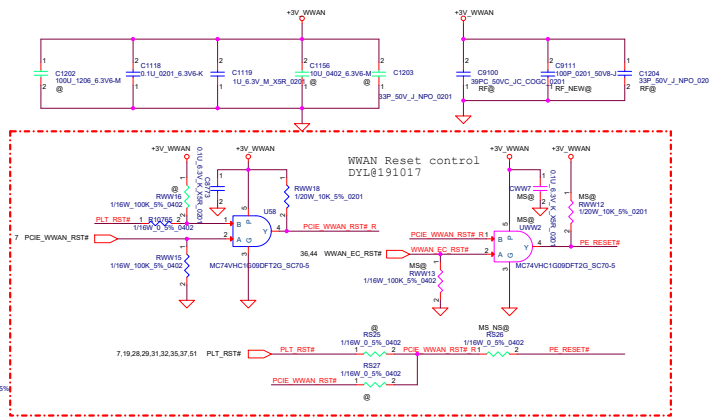
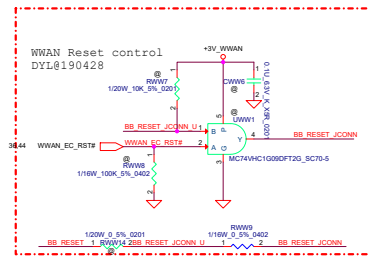
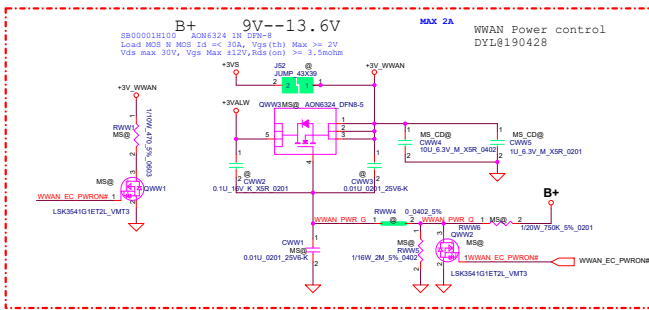


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Issued Date		Deciphered Date		BLANK	
2018/8/9		2018/8/9			
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				Small	Sideswipe&Jazz AMD2
				Date	Rev
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				Sheet	31 of 68



5		4		3		2		1	
D									
C									
B									
A									





TYPE-B NGFF CARD FOR WWAN

2.00mm Connector

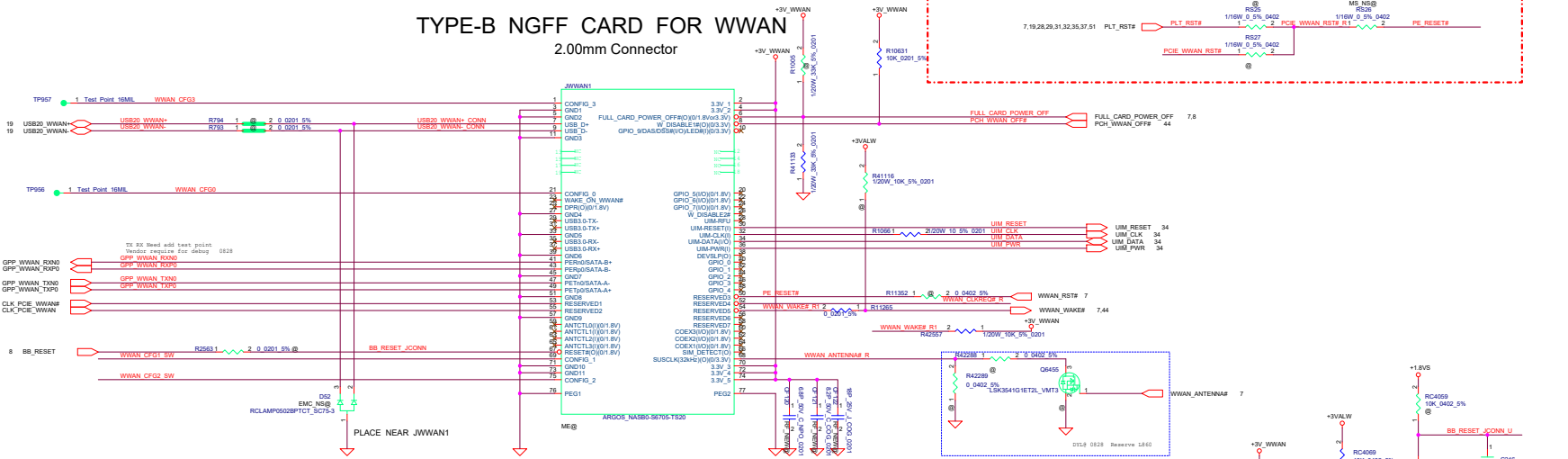


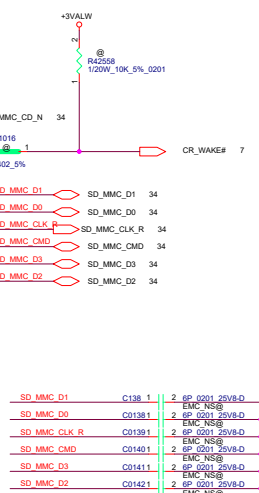
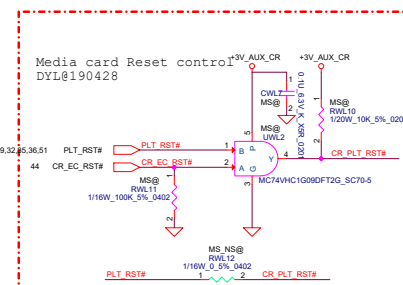
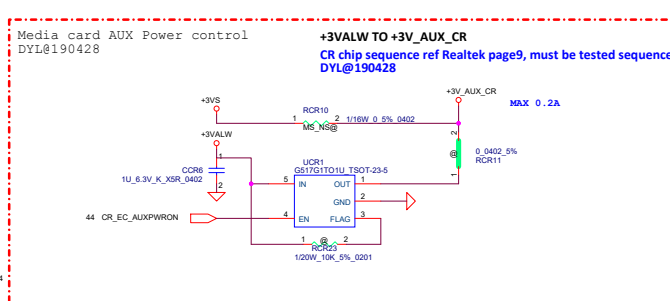
TABLE:

Module Configuration Decodes					Module Type and Main Interface	Port Configuration
State #	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	NC	GND	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - USB 3.0	0
5	GND	NC	GND	NC	WWAN - USB 3.0	1
6	GND	NC	NC	GND	WWAN - USB 3.0	2
7	GND	NC	NC	NC	WWAN - USB 3.0	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	RFU	N/A
15	NC	NC	NC	NC	No Module Present	N/A

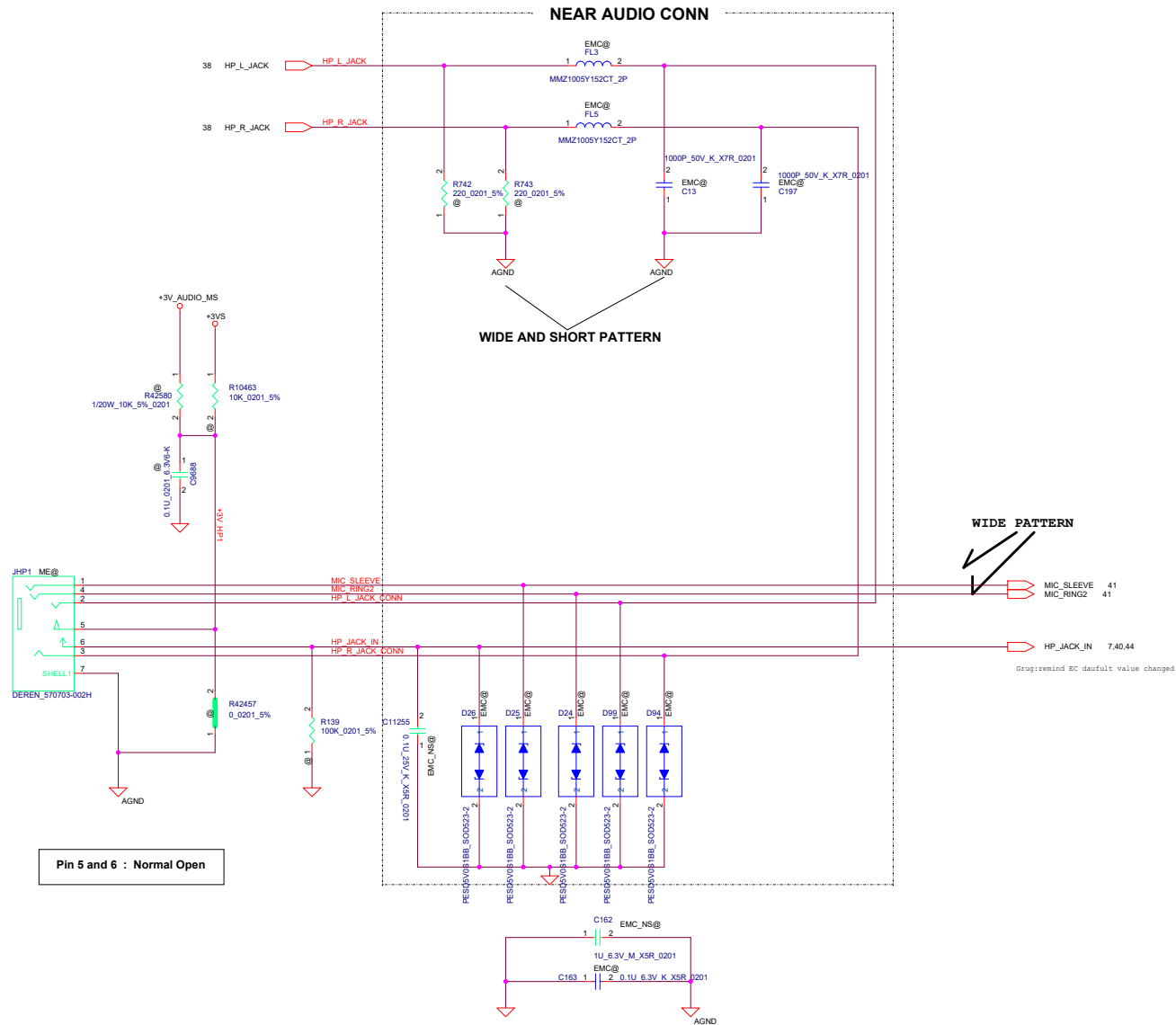
TABLE:

	Module Configuration Decodes			
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)
Fibcom L830-EB	GND	NC	GND	GND
Sierra EM7565	GND	NC	NC	GND
2242 PCIe SSD	GND	GND	GND	NC
				Detect -WWAN_SSD_DTCT

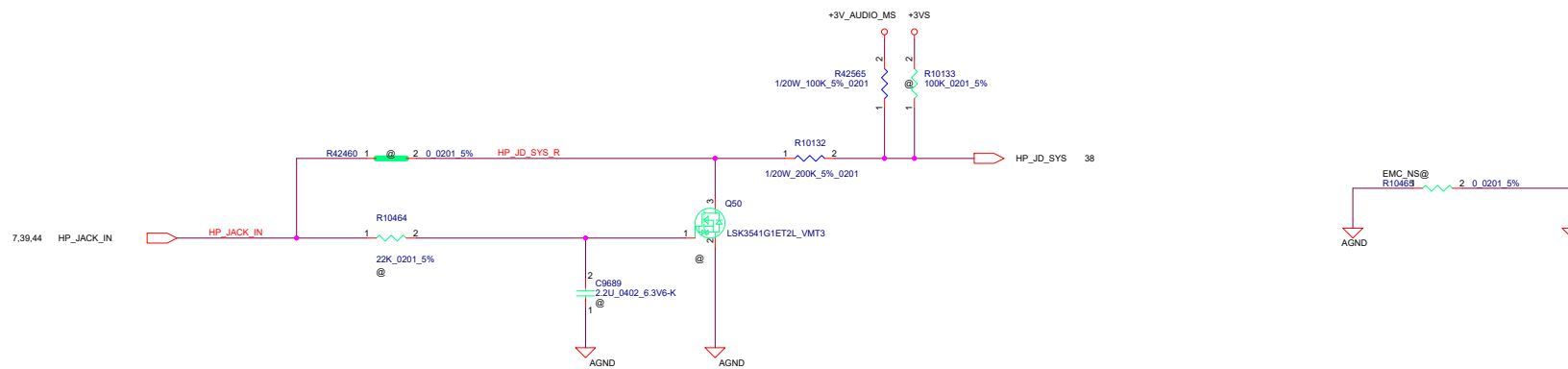
Vcc	3.32V					
R10955	1.992V	1.686V	1.533V	2.548V	2.215V	3.32V
DEVICE_DETECT1#	V	V	V	X	X	X
SSD_DETECT#	V	V	V	X	X	X
WWAN_DTCT#	X	X	V	X	V	X
Configuration	Only 2280680	228042242 SSD	2280880WWAN	Only 2242930	Only WWAN	No Device

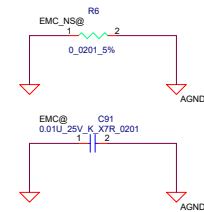
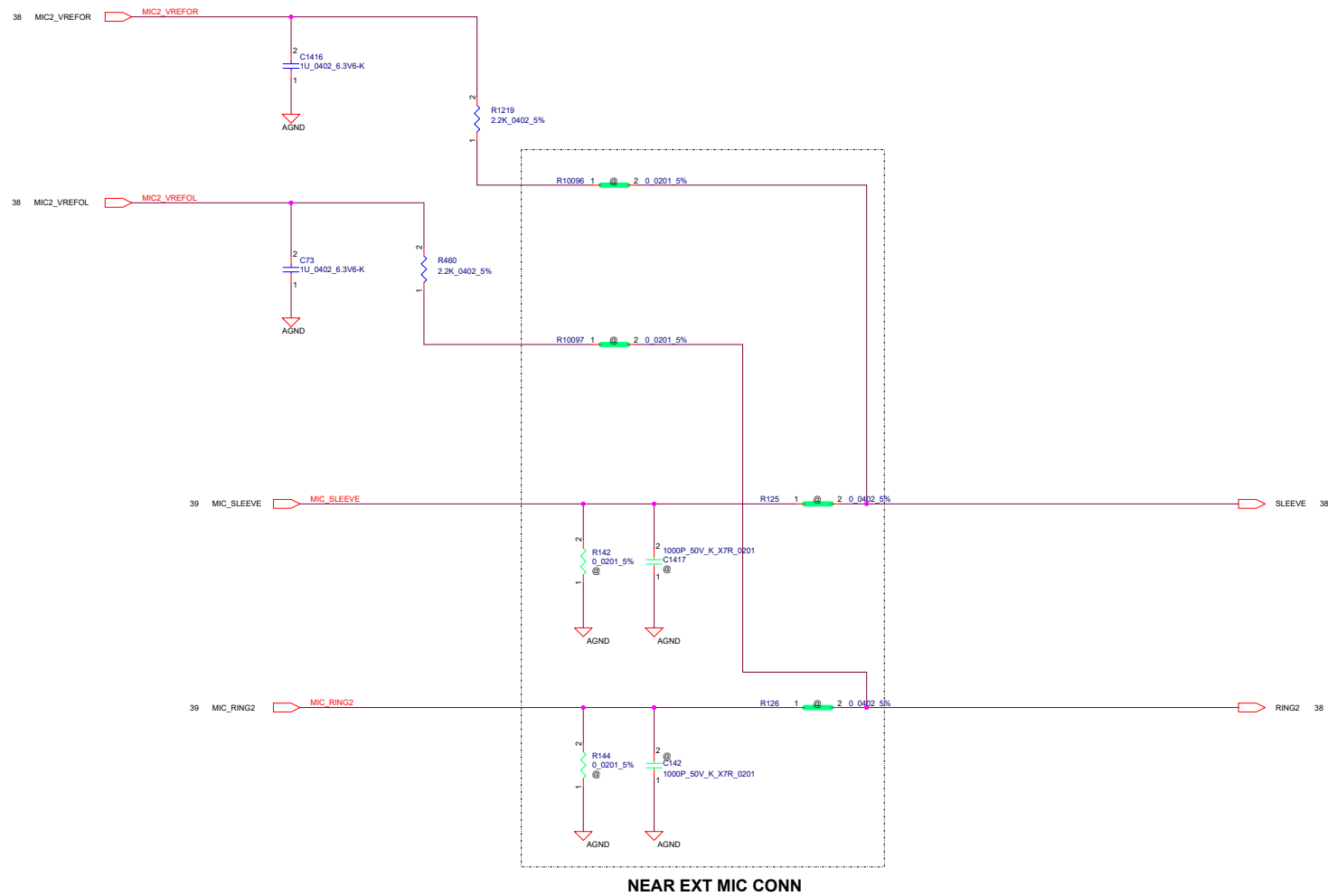


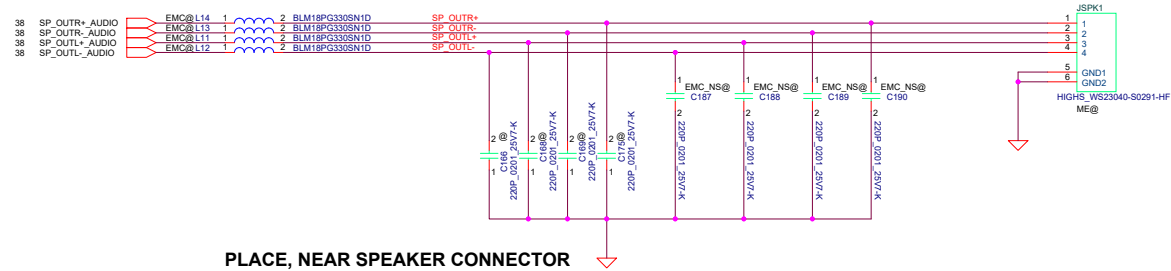
Part Number	Vendor
SA000077K00	RTS5232S-GR REALTEK
SA00009JG00	GL9750-OIYL3 GENESYS



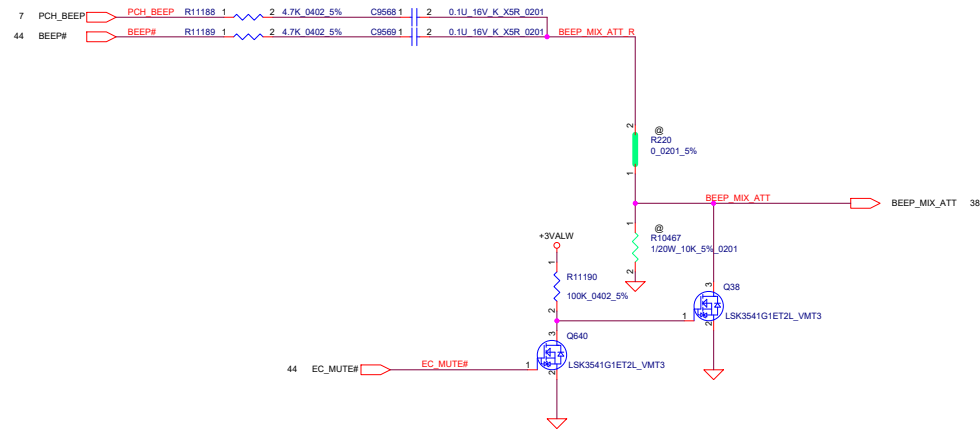
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Issued Date	2018/8/9	Deciphered Date	2018/8/9	AUDIO CONNECTOR	
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				Date	Rev
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				Sheet	35 of 68







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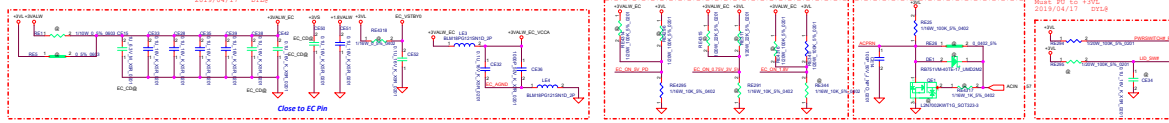


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Issued Date	2018/8/9	Deciphered Date	2018/8/9	AUDIO BEEP
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				Document Number: Sideswipe&Jazz AMD2
				Date: Saturday, April 04, 2020
				Sheet: 43 of 68
				Rev: 1.0



EC Decoupling for ELPM function reserve

2019/04/17 DVS8

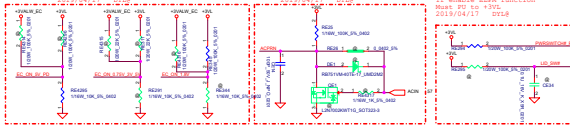


Close to EC Pin

Close to EC Pin A1

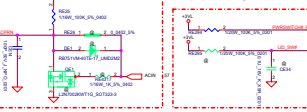
PMU Decoupling for ELPM function reserve

2019/04/17 DVS8



ACIN for ELPM function reserve

2019/04/17 DVS8



LD4PMU_SWITCH

If enable ELPM function

Need P1 to P102

2019/04/17 DVS8



EC Decoupling for ELPM function reserve

2019/04/17 DVS8



Close to EC Pin

Close to EC Pin A1

PMU Decoupling for ELPM function reserve

2019/04/17 DVS8



ACIN for ELPM function reserve

2019/04/17 DVS8



LD4PMU_SWITCH

If enable ELPM function

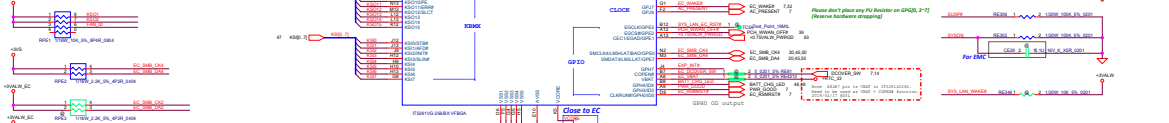
Need P1 to P102

2019/04/17 DVS8



EC Decoupling for ELPM function reserve

2019/04/17 DVS8

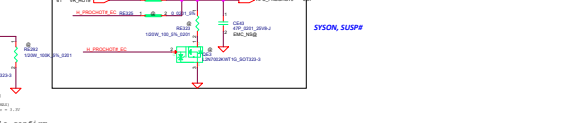


Close to EC Pin

Close to EC Pin A1

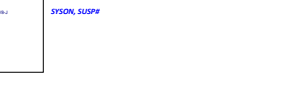
PMU Decoupling for ELPM function reserve

2019/04/17 DVS8



ACIN for ELPM function reserve

2019/04/17 DVS8



LD4PMU_SWITCH

If enable ELPM function

Need P1 to P102

2019/04/17 DVS8



EC Decoupling for ELPM function reserve

2019/04/17 DVS8

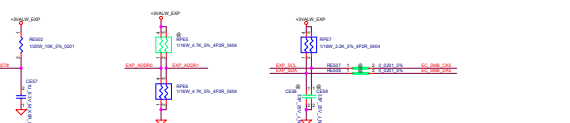


Close to EC Pin

Close to EC Pin A1

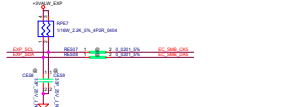
PMU Decoupling for ELPM function reserve

2019/04/17 DVS8



ACIN for ELPM function reserve

2019/04/17 DVS8



LD4PMU_SWITCH

If enable ELPM function

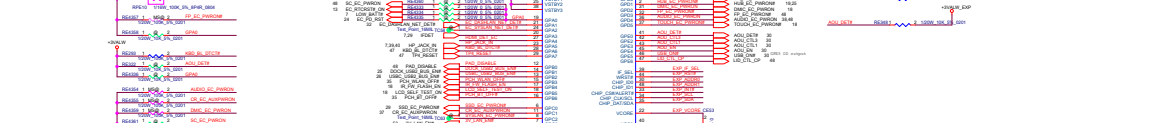
Need P1 to P102

2019/04/17 DVS8



EC Decoupling for ELPM function reserve

2019/04/17 DVS8

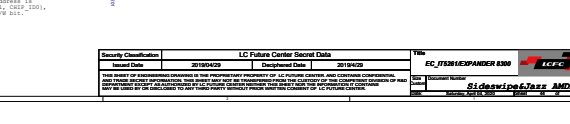


Close to EC Pin

Close to EC Pin A1

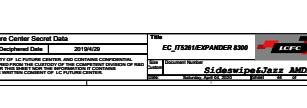
PMU Decoupling for ELPM function reserve

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ACIN for ELPM function reserve

2019/04/17 DVS8



LD4PMU_SWITCH

If enable ELPM function

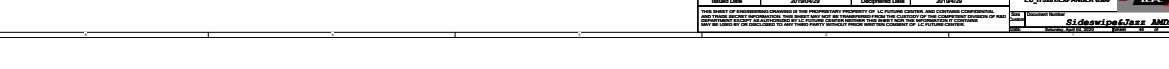
Need P1 to P102

2019/04/17 DVS8



EC Decoupling for ELPM function reserve

2019/04/17 DVS8



Close to EC Pin

Close to EC Pin A1

PMU Decoupling for ELPM function reserve

2019/04/17 DVS8

ACIN for ELPM function reserve

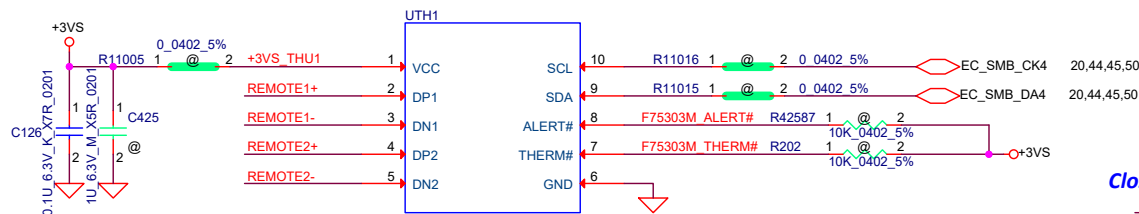
2019/04/17 DVS8

LD4PMU_SWITCH

If enable ELPM function

Need P1 to P102

2019/04/17 DVS8



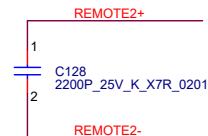
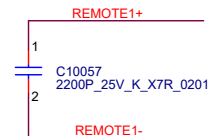
F75303M_MSOP10

Address 1001_101xb

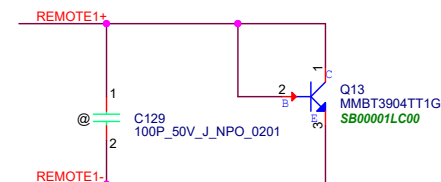
Internal pull up 1.2K to 1.5V

R for initial thermal shutdown temp

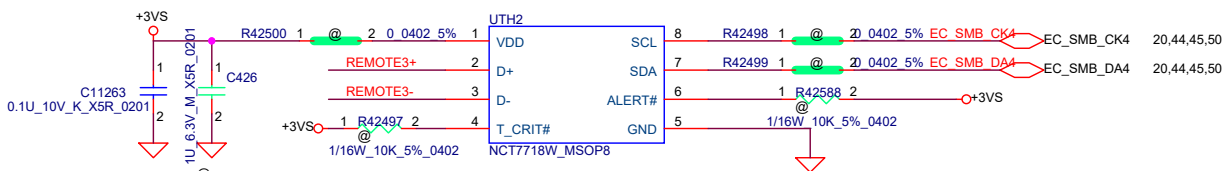
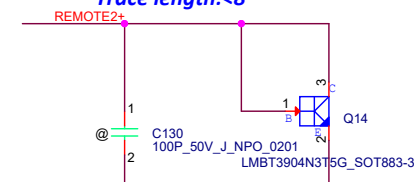
Close to UTH1



Close to FIN



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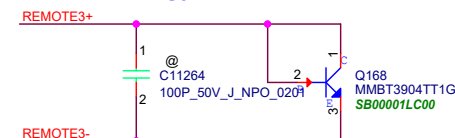
NCT7718W I2

C/ SMBus™ address is 1001100xb (x is R/W bit).


Close to UTH2

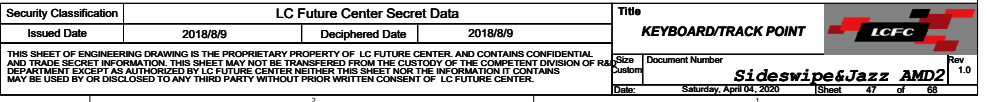


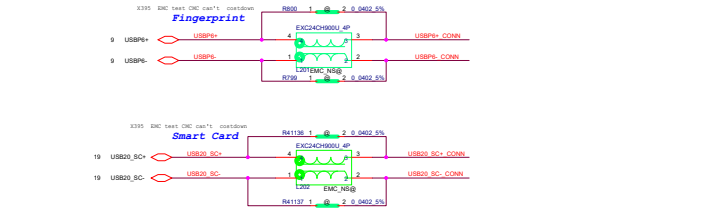
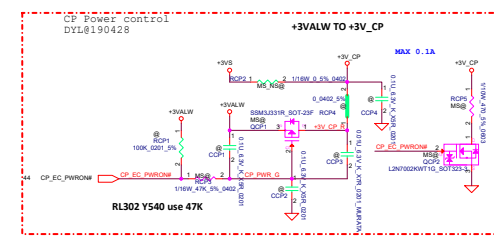
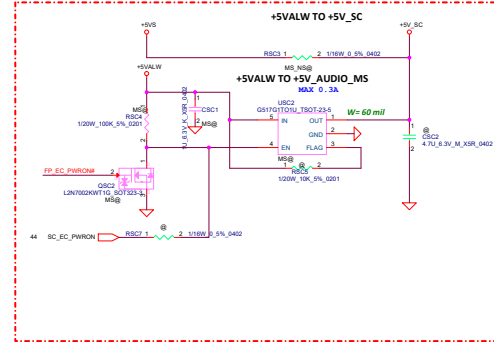
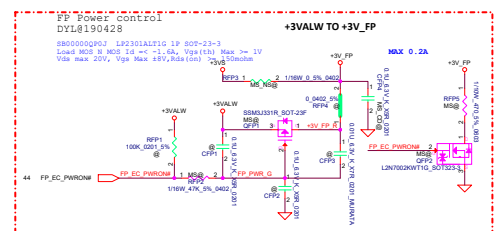
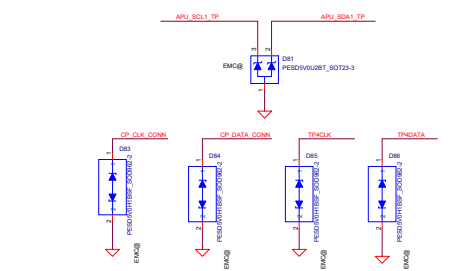
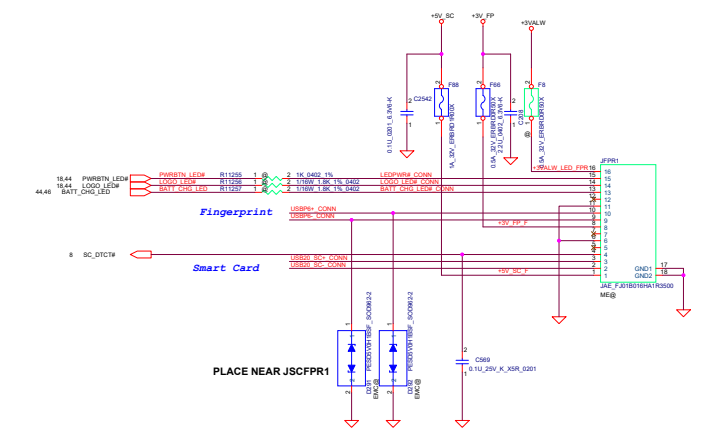
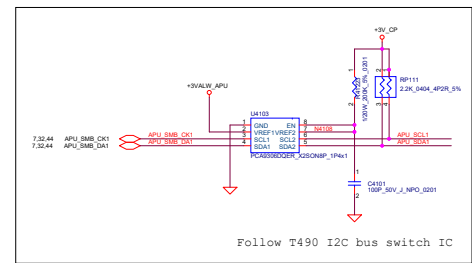
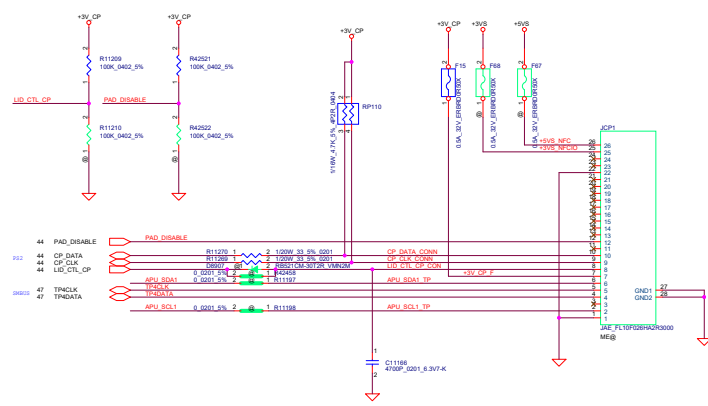
Near

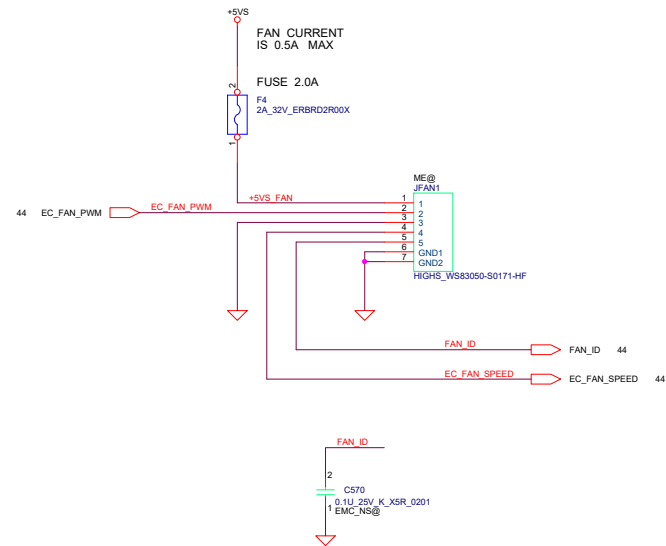


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

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Issued Date		Deciphered Date		THERMAL SENSOR			
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				5			
				Date:	Saturday, April 04, 2020	Sheet 45 of 68	



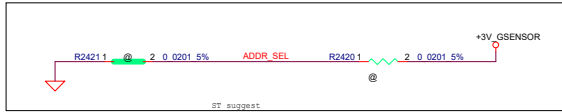




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Issued Date	2018/8/9	Deciphered Date	2018/8/9	Size	Document Number
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			Date	Saturday, April 04, 2020	1.0
			Sheet	49	of 68



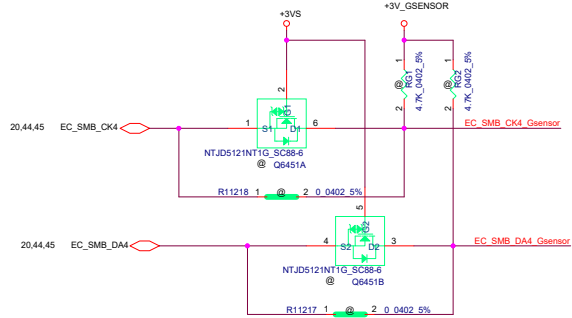
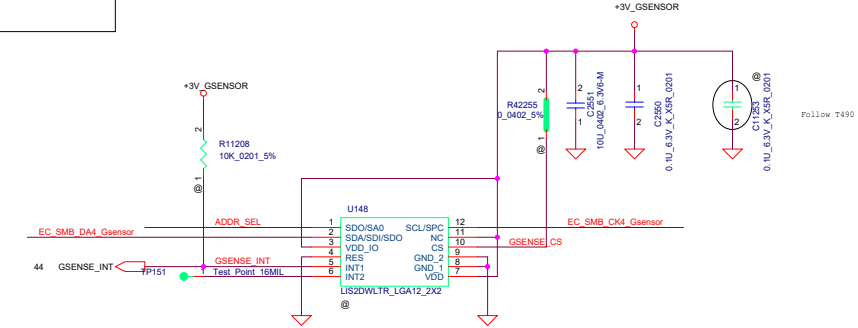
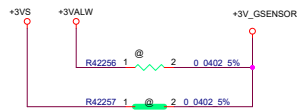
Sideswipe&Jazz AMD2



TABLE

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

TABLE of G-Sensor (U148)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00



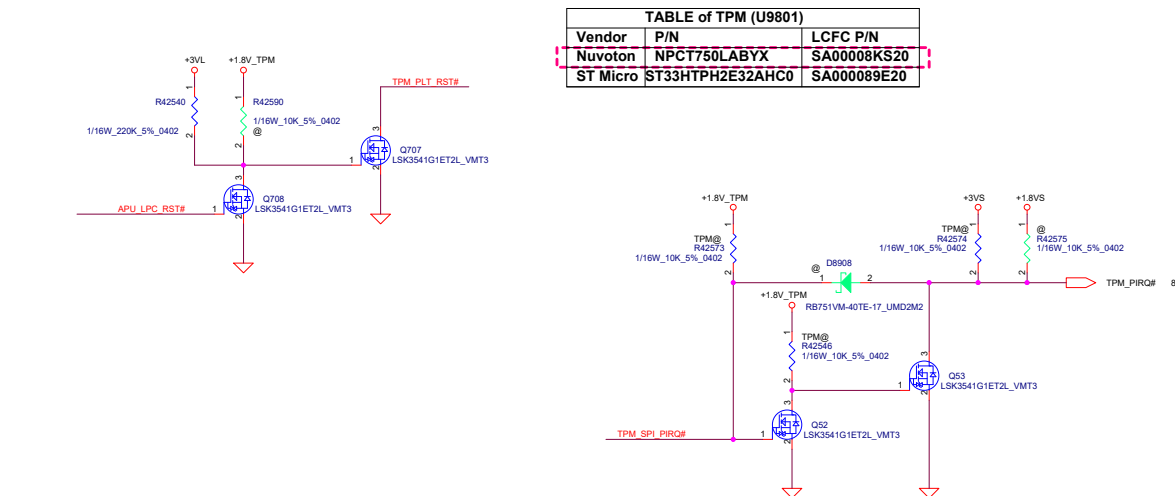
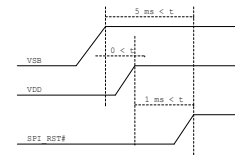


TABLE of TPM (U9801)		
Vendor	P/N	LCFC P/N
Nuvoton	NPCT750LABYX	SA00008KS20
ST Micro	ST33HTPH2E32AHC0	SA000089E20

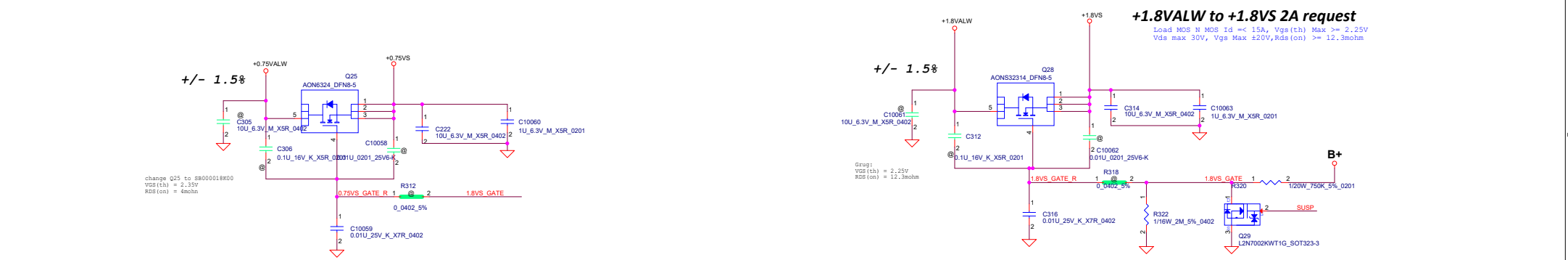
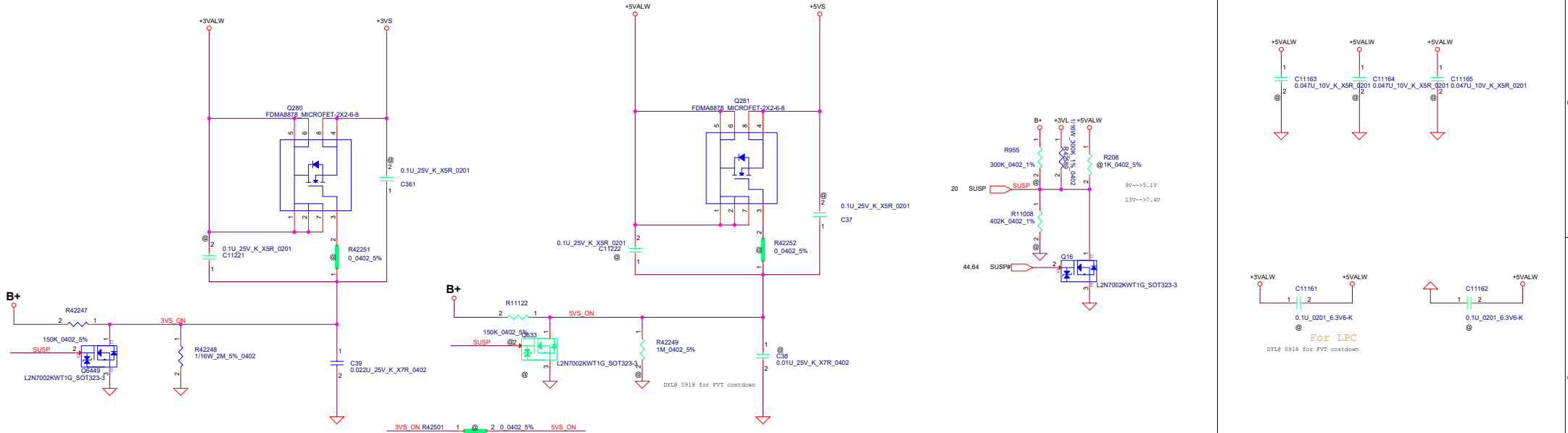
NOTE:
Check timing sequence in SDV phase.



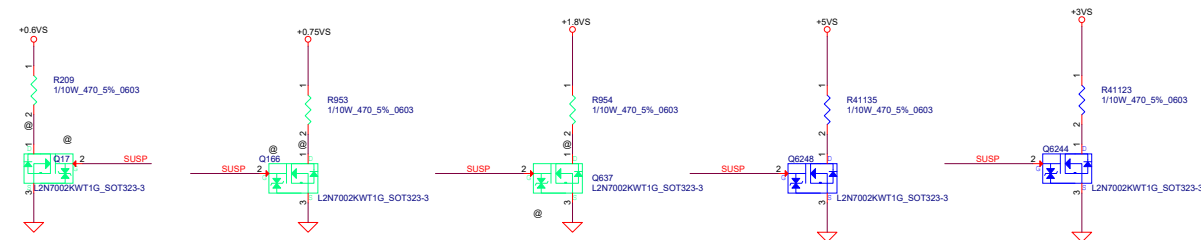
- NOTE:
- 1) It is recommended to connect the TPM to the system's standby voltage to improve performance.
 - 2) SPI RST# must be asserted for at least 5 msec after VSB power-up.
 - 3) VSB may come up anytime before VDD power-up, but not after VDD power-up.
 - 4) SPI RST# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.


TABLE

Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LABYX	ST Micro ST33HPTH2E32AH
1	VDD	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	GPIO	GPIO/PP	PP
5	NC	NC	NC
6	GPIO	GPIO3	NC
7	GPIO	NC	GPIO
8	VDD	VHIO	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI#/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC

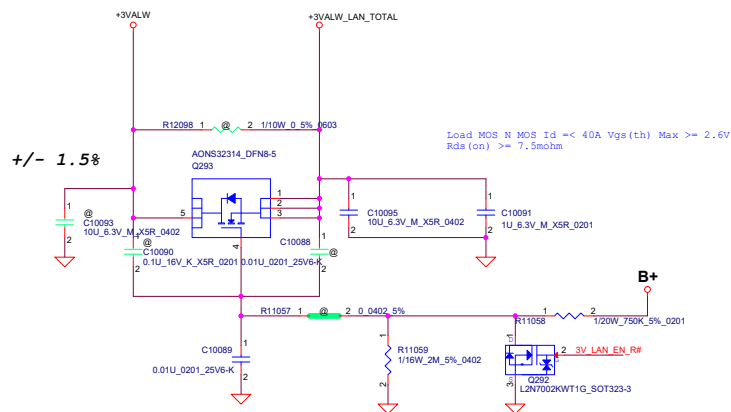
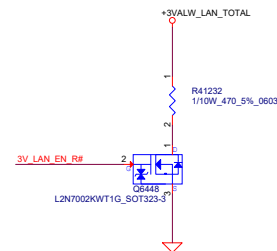
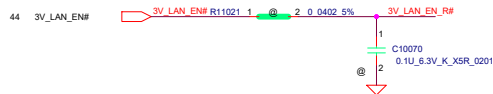


For DisCharge

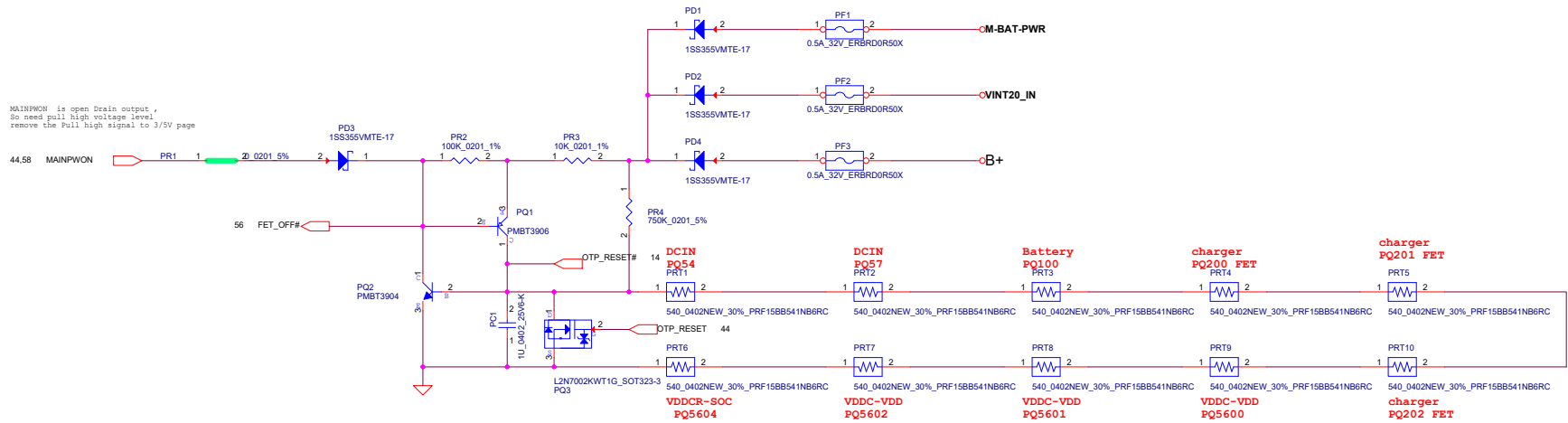


Security Classification				LC Future Center Secret Data				Title							
Issued Date		2018/8/9		Deciphered Date		2018/8/9		LOAD SW 1							
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										Date	Saturday, April 04, 2020	Sheet	52	of	68

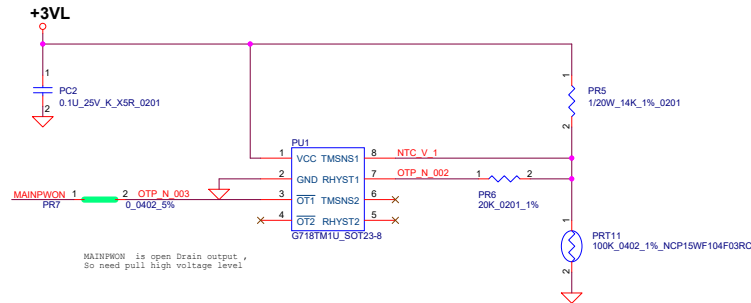




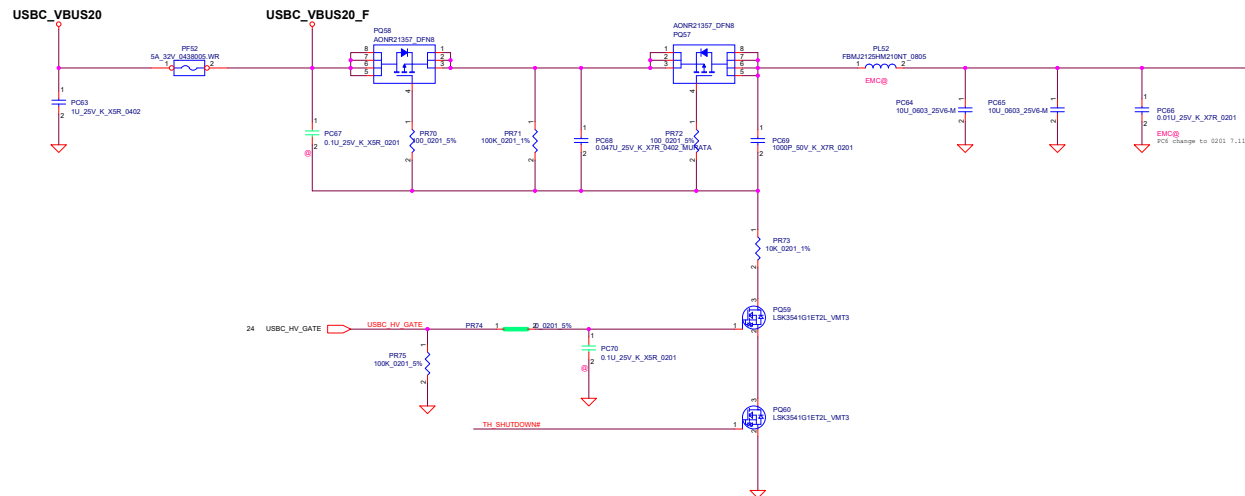
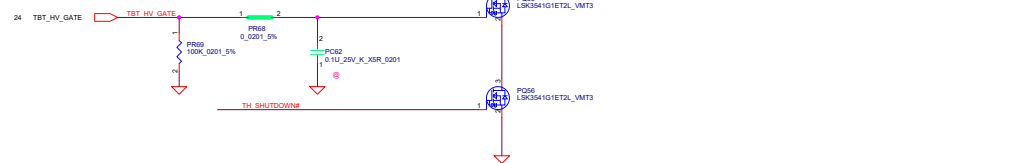
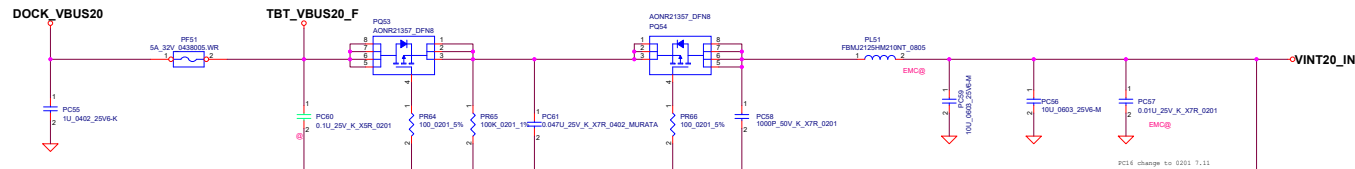
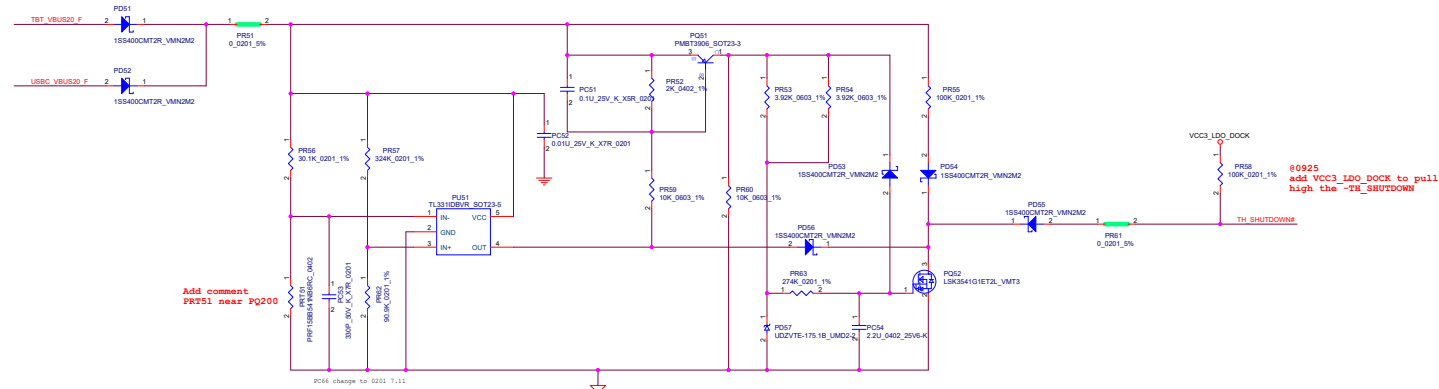
MAINPWON is open Drain output ,
So need pull high voltage level
remove the Pull high signal to 3/5V page

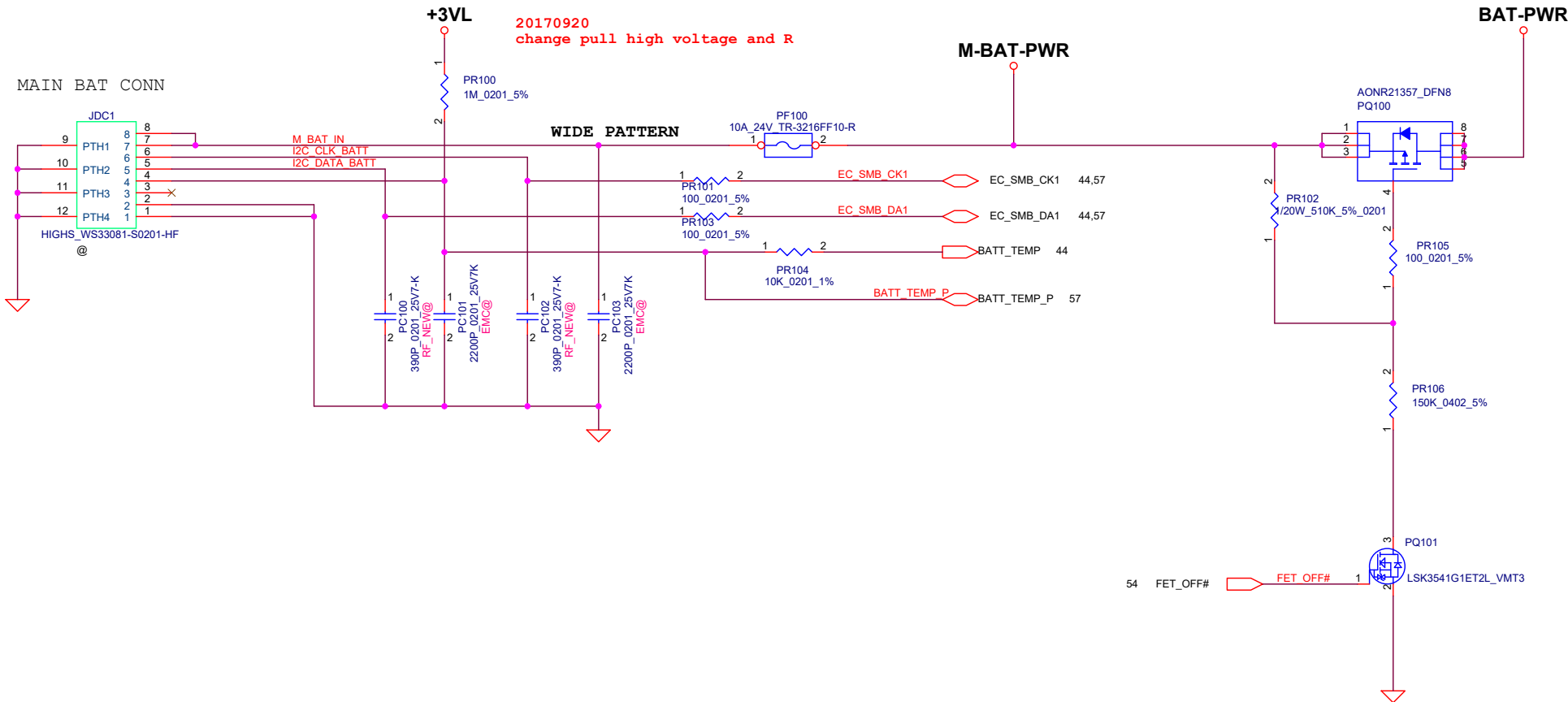



540_0402NEW_30%_PRF15BB541NB6RC
25~100Degree
0.54@25 Degree
1.2*0.54*k@85Degree
2*0.54 k@100 Degree
20*0.54 k@120Degree
100*0.54 k@130Degree
350*0.54 k@140Degree
Vbattery min =9V,Vbattery max =12.6V
Vthreshold min=0.65V,Vthreshold min=0.85V,
TotalR (PTC)*(VBatt-1.25)/(TotalR (PTC)+750)=0.65V
TotalR (PTC)max=59.8K~==110 times 0.54 k
TotalR (PTC)min=43.72K~==80times 0.54 k
Normal run 3Dmark
the max T maybe 85 Degree
the total R PTC= 1.2*0.54*10=12*0.54 k
if only one PTC over 130 degree,
the total PTC is 100*0.54K+11*0.54k,>80*0.54K
and over the min Vthreshold,and active the OTP
if only one PTC over 140 degree,
the total PTC is 350*0.54K>>80*0.54K
,can over the min Vthreshold
and active the OTP
so,the OTP function is ok



PRT11 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



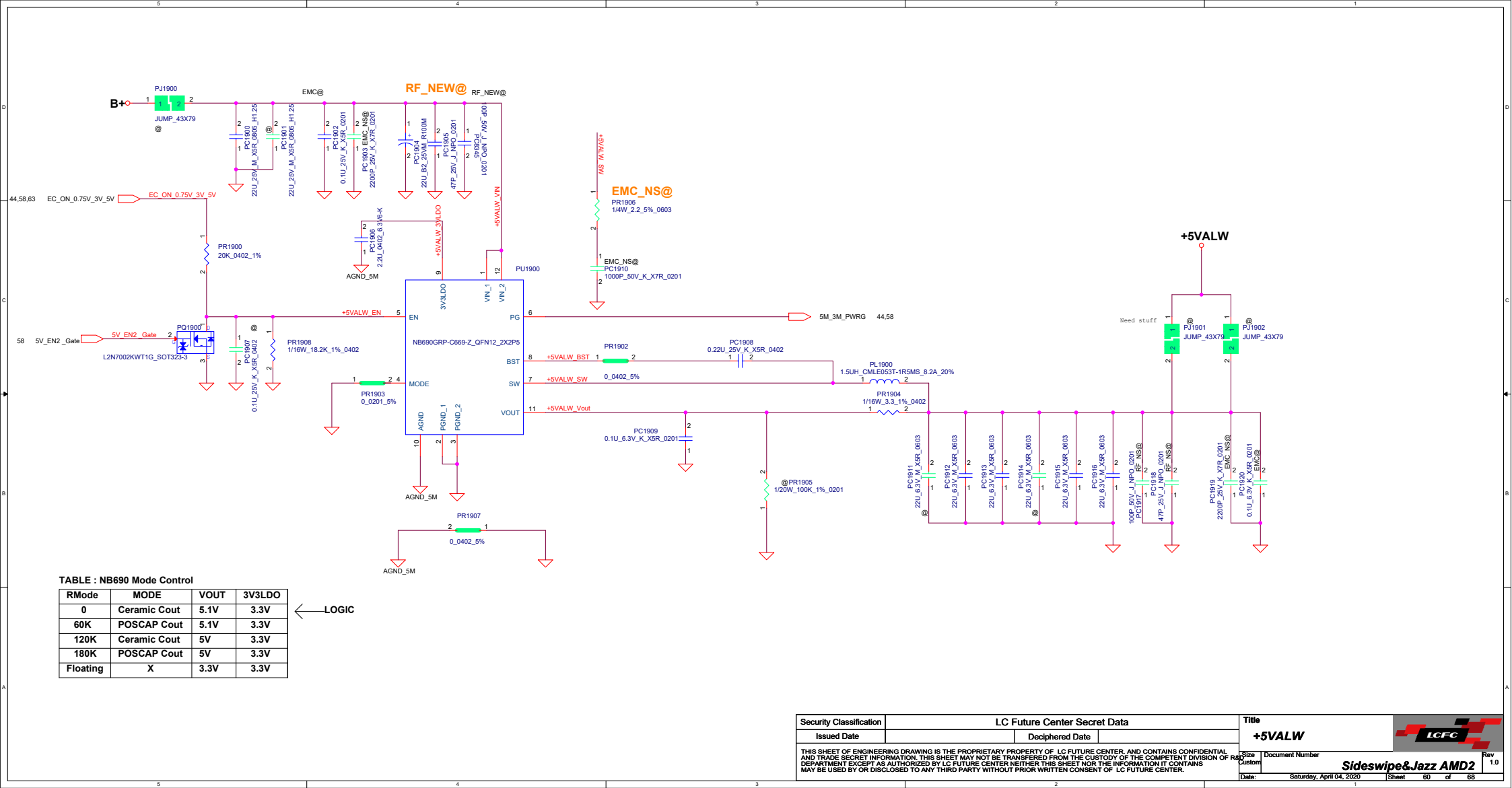


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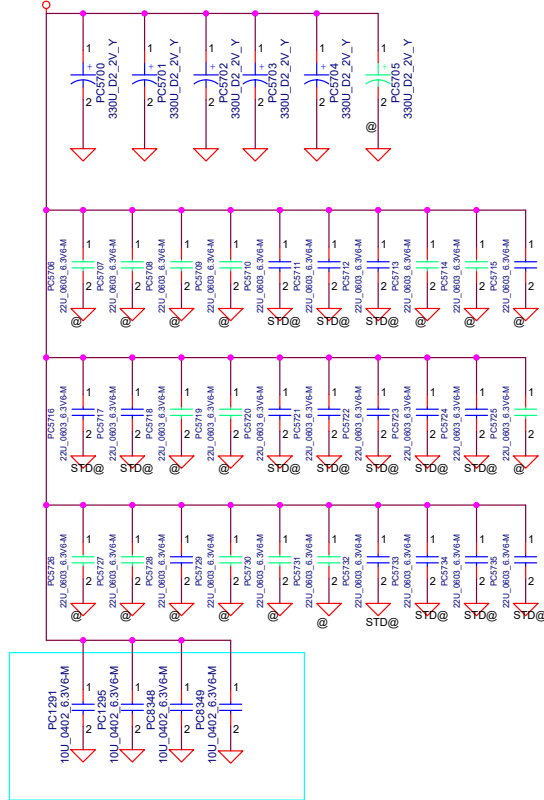
PCB layout of the BQ76941 evaluation board. The layout shows the internal circuitry, components, and routing. Key components include the BQ76941 IC, various capacitors, resistors, and a MOSFET. The layout is annotated with component values, pin numbers, and routing notes. A green box highlights a routing note: "Keep these two signals as pair routing". A red dashed box highlights a component change note: "20170918Snubber Cap Change Follow II". The layout is symmetrical on top and bottom.

← LOGIC

# of CELL	VCELL_PRES	PR154
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

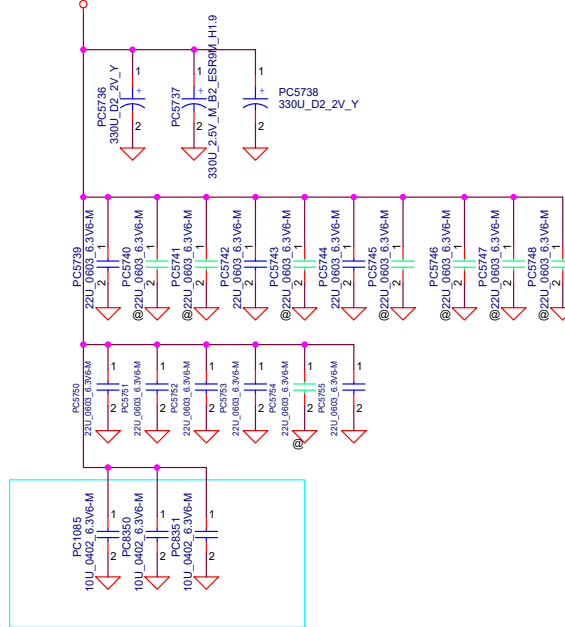


+VDDCR_CPU



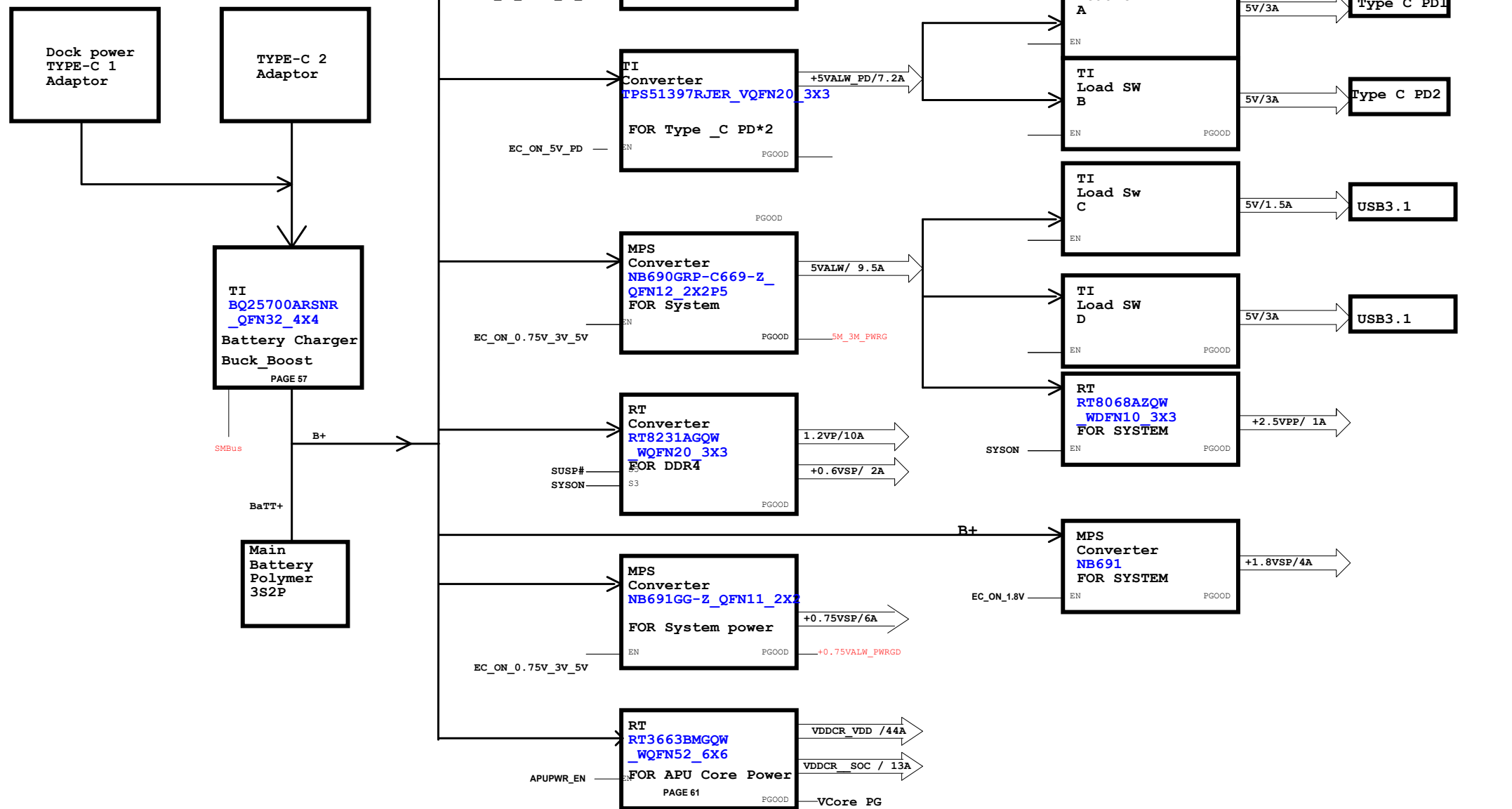
Note
330uF/9mohm*2pcs
22uF/0603*20pcss

+VDDCR_SOC



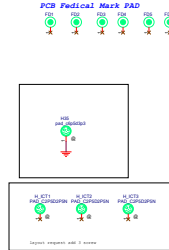
330uF/9mohm*2pcs
22uF/0603*12 pcss

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56G50A@B 22211	56G50A@B 22212	56G50A@B 22213	56G50A@B 22214	56G50A@B 22215	56G50A@B 22216	56G50A@B 22217	56G50A@B 22218	56G50A@B 22219
SAMUNG DB	HYNX DB	MICRON DB	SAMUNG D16G	HYNX D16G	MICRON D16G	SAMUNG D32G	HYNX D32G	MICRON D32G
X7649@1027	X7649@1028	X7649@1029	X7649@1030	X7649@1031	X7649@1032	X7649@1033	X7649@1034	X7649@1035



Samsung D8G

Hynix D8G

Micron D8G

Samsung D16G

Hynix D16G

Micron D16G

Samsung D32G

Hynix D32G

Micron D32G